GROWTH OF GERMANIUM NANOWIRES FOR THERMOELECTRIC APPLICATIONS

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Contents

Summary

This research focuses on the growth and fabrication of germanium nanowires for the measurement of their resistance and Seebeck coefficient, an important parameter in the thermoelectric performance of a device. Although silicon is known as a poor thermoelectric material, it was shown that silicon in the form of nanowires exhibits thermoelectric performance comparable to the best thermoelectric devices currently in commercial use. This is extremely significant as silicon is widely available and immense knowledge and know-how are available regarding its processing. Naturally comes the question of whether materials somewhat similar to silicon, such as germanium, would exhibit similar interesting thermoelectric behavior when engineered in the form of nanowires. Amongst several ways to grow germanium nanowires, the vapour transport method was chosen, by using a conventional furnace tube. This setup is certainly the simplest to grow nanowires by evaporation, as it uses a solid nanopowder source instead of a gas source. The counterpart is the difficulty in the control of the growth parameters. The literature on growth control of semiconductor nanowires was extensively reviewed. Very little data is available on the growth and control of the characteristics of germanium nanowires using a furnace. Most research focuses on growth using the more traditional chemical vapour deposition with a gas source. These systems allow a high level of control and are by design very different from furnace tubes. Therefore, an important work of translation of

the available data was necessary to be put to use in our system. Following attempts on stainless steel substrates, most of the growth effort was spent on more traditional silicon substrates. Next, the challenge of growing wires that can be integrated into a spun-on oxide matrix was overcome. Each step of incremental adaptation of the growth parameters is presented. It was found that despite the high melting point of germanium, evaporation of the germanium powder source occurs even at temperatures 100°C below the melting point of solid germanium. Lowering the source temperature to this extent allows one to control significantly the growth rate. With no surprise whatsoever, reducing the growth duration was also critical, though it was beneficial only after the reduction of the source temperature to allow for fine tuning of the growth rate. Reducing the source temperature was also necessary to control the growth rate, it is to come in order as the third fine tuning option. Next, a study of the integration of the resulting nanowires is presented, with a particular emphasis on the surface irregularity due to the presence of obstacles (nanowires) in the oxide matrix layer. Finally, the qualitative usability of the alternating current-polarity Seebeck measurement technique is studied. The inherent challenges and limitations of this technique are presented, and an alternative to the alternating current-polarity method is introduced.

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Symbols

S	Seebeck coefficient
α	Seebeck coefficient
ZT	thermoelectric figure of merit of a device
zT	thermoelectric figure of merit of a material
σ	electrical conductivity
ρ	electrical resistivity
μ	denotes the electrical mobility or the the “micro” unit prefix
κ	dielectric constant
k	thermal conductivity
V	denotes a voltage variable or the volt unit
V_{TOT}	total voltage measured onto a device
V_{IR}	resistive voltage
V_{IR}	resistive voltage
$\mathrm{V}_{IR}(I^-)$	resistive voltage induced by the application of a negative current
$\mathrm{V}_{IR}(I^+)$	resistive voltage induced by the application of a positive current

R	electrical resistance
R_{th}	thermal resistance
Q	heat load
T	Temperature
K	Kelvin
$^{\circ}C$	degree Celcius
W	watt
L	Lorentz factor, $L = 2.4 \times 10^{-8}$ $J^2.K^2.C^{-2}$ for free electrons
h	PlanckÕs constant, $h = 6.626068 \times 10^{34} m^2.kg.s^{-1}$
m^*	effective mass
e	elementary charge, $e = 1.60217646 \times 10^{19} C$
eV	electron-volt
I	refers to an electrical current, or to the iodine element
Å	angstrom
Ω	ohm
ΔV	voltage difference
ΔT or Δ_T	temperature difference
Si	silicon
SiO_2	silicon dioxide
Ge	germanium
GeH_4	germane
Ge_2H_6	digermane
B_2H_6	diborane
PH_3	phosphine
TEGe	tetraethylgermane
Sb	antimony

Bi	bismuth
Te	tellurium
Pb	lead
Au	gold
P	phosphorous
H	hydrogen
Fe	iron
Al	aluminum
Ni	nickel
In	indium
Ti	titanium
Bi_2Te_3	bismuth telluride
0D, 1D, 2D, 3D	denotes respectively zero-dimensional, once-dimensional, two-dimensional and three-dimensional

Abbreviations

NW	nanowire
NWs	nanowires
TE	thermoelectric
SOG	spin-on-glass
CCD	charge-coupled device
PGEC	phonon-glass/electron-crystal
VLS	vapour-liquid-solid
CVD	chemical vapour deposition
SEM	scanning electronic microscope
TEM	transmission electronic microscope
VSS	vapour-solid-solid
XRD	x-ray diffraction
sccm	standard cubic centimeters per minute
CMOS	complementary metal-oxide-semiconductor
IL	interference lithography
AAO	anodized aluminum oxide
PS	polystyrene spheres
EBL	electron-beam lithography
APTS	aminopropyl trimethoxysilane
PVD	physical vapour deposition
IPA	isopropyl-alcohol
rpm	revolutions per minute
SMU	source and measurement unit
SS	stainless steel
CMP	chemical and mechanical polishing

CSV	comma-separated value

1. Introduction

1.1 Background

Thermoelectric (TE) materials convert heat into electric current, and vice versa. More precisely, thermoelectric conversion relies on a temperature gradient, a difference between hot and cold areas of a device. In such materials, heat flowing from the hot side to the cold side creates a current flow, which can be used to power a device or stored for subsequent use. The process is reversible, and thus applying electrical power generates a temperature gradient across the sample. This effect is called the Seebeck effect.

The efficiency of this thermoelectric conversion is measured by the figure of merit $ZT = \frac{S^2 T}{\rho k}$ where S, T, ρ and k are respectively the Seebeck coefficient, temperature, resistivity and thermal conductivity. The Seebeck coefficient, also referred to as the thermopower, is a key value and is defined by the ratio of voltage to temperature gradient, $S = -\frac{\Delta V}{\Delta T}$. The sign of S depends on the majority charge carriers involved; a positive sign for p-type material with holes as the majority carriers and a negative sign for n-type material with electrons as the majority carriers.

Since the discovery of the Seebeck effect by the inventor of the same name

in 1821 [1]. Thermoelectric materials have improved gradually, until the 1950s when the basic science of thermoelectrics became well established. By the 1960s, the material bismuth telluride Bi_2Te_3 was developed for commercialization. Until the 1990s, little interest was shown for thermoelectric materials. Only incremental improvement were observed with the advent of a new alloy family, $(Bi_{1-x}Sb_x)_2(Se_{1-y}Te_y)_3$, which is not quite a breakthrough however.

It is only in the 1990s that theoretical work predicted that nanostructuring thermoelectric materials would greatly increase their performance, thus creating interest in the field. Various forms of nanostructuring have been explored, typically superlattices and nanocomposites (nanostructures embedded in a host material). Among these nanostructures, nanowires represent a common form of one-dimensional nanostructures. Nanowires are indeed one of the more interesting structures in terms for thermoelectric applications as they present strong quantum confinement as compared to two-dimensional (2D) superlattices, while maintaining structural continuity in one dimension, thus allowing for transport phenomena.

Although bulk silicon (Si) at room temperature has a ZT of 0.01, it was recently found that the nanoscale geometries of the silicon wires reduce the thermal conductivity by about 100 times. Hochbaum *et al.* (2008) [2] quotet a ZT value of 0.6 for their silicon nanowires, while Boukai *et al.* (2008) [3] reported a ZT of about 0.4 at 300 K, and around 1 at 200 K. This makes silicon nanowires comparable to the best bulk thermoelectric materials such as bismuth tellurides. Silicon, the basic material of semiconductor electronics, is readily available, cheap and has immense infrastructure and know-how for its production.

However, it remains important to search for other materials that may have comparable or better performance than Si. In this projection, one may consider the use of germanium (Ge). In the bulk state, Ge has about three times higher carrier mobilities than silicon and a Bohr radius that is about five times larger. Like Si, it is also compatible with high dielectric constant materials.

1.2 Motivation of project

Although thermoelectric (TE) composites, such as nanowire-based TE devices, have not yet been commercially used, the potential uses are numerous, part of which lies on the current applications of bulk TE devices.

By aiming at providing better energy performance, the TE composite research is particularly exciting because it utterly supports for a better use of energy. While reducing the power consumption of cooling systems, a newly competitive TE technology like semiconductor nanowires may also attempt to harvest non-avoidable energy wastes that present themselves in the form of heat.

Heat engines More than 90% of the world's electricity originates from heat engines with average efficiency of 30 to 40%. A subsequent part of the waste energy is heat [2]. The ideal solution would undoubtedly be to replace heat engines by environment-friendly and high-performance electrical plants. However, using TE as a transitional technological solution would valorize one of the largest energy wastes on the planet.

Fuel engines Cars, like other fuel engines, lose about two thirds (66%) of their energy into heat. While considerable efforts are made to reduce wastes in a motor, it remains that by design, a fuel engine is meant to produce unnecessary waste heat. Supposing that a significant part of the waste is converted into electricity and used to replace a part of the fuel-converted energy, fuel consumption could therefore be reduced. The car manufacturer BMW succeeded in proving this proof of concept by integrating a thermoelectric generator onto the exhaust pipe of a prototype model. Although only 200 W were generated, research is being carried out to reach 1000 W, which would represent a reduction of about 5% of the car's consumption [4].

Solar Cells Nanostructures made from BiSbTe would have a better efficiency at converting solar heat into electricity than solar cells fabricated with amorphous silicon to convert solar energy (light) to electricity [5].

Computers Other applications include harversting the heat from electronic chips, the efficiency of which is reported to be about 1% [6]. While cooling the chips preserves them from accelerated heat damage, TE modules integrated onto electronic chips would also retrieve heat for potential re-use in the computer.

Cooling systems Although the most interesting use of TE devices is energy harvesting, the commercial current reality is that most applications are based on converting electricity into cooling power [5]. Fortunately, achieving good performance in heat harvesting is equivalent to achieving good performance in cooling. Current applications include coolers for CCD detectors of infrared cameras or laser diodes and other scientific measuring equipment, and also in popular equipment such as refrigerators, cold water public taps, high-tech picnic baskets and seats of luxury cars [7].

1.3 Objectives and Scope of the study

The main objective of this study is to explore growth of Ge nanowires that exhibit TE-relevant characteristics. Ultimately, an important aspect of this study involves fabricating an experimental device in order to attempt measuring the Seebeck coefficient of Ge NWs embedded in an oxide matrix.

The variety of parameters that can affect the growth of Ge NWs by vapour transport can be puzzling. This study exhibits through experimental work the complex interactions and their use in order to obtain TE-relevant NWs. The set of desired characteristics for TE-relevant NWs is mainly discussed in the literature review, and is used as a guide throughout the experiments.

Then, different experiments to integrate the desired NWs are conducted. Integration is a particularly difficult step and many defects can result from this process. The present work proposes solutions to address this issue.

Finally, the process of fabricating a TE device structure is exposed. The electrical measurements aiming at extracting the Seebeck coefficient of the device are analyzed and discussed.

1.4 Organisation of thesis

Chapter 2 presents a literature review of both theoretical and experimental aspects of this work. It begins with a review of theoretical knowledge on low dimensionality thermoelectrics and the recent proofs of concept on silicon nanowires (NWs). Explanation on the motivations to explore the TE performance of Ge NWs are given. Then, the growth methods of Ge NWs are reviewed. A particular focus is brought on the effect of different growth parameters on the NW characteristics. This is followed by sections presenting the post-growth processes. Firstly, the rationale to specify the integration material is explained, which is followed by a description on possible candidate materials and processes before analyzing the state-of-the-art techniques used in scientific research. Secondly, the techniques to measure the resistivity of the device are described. This measurement is critical for the extraction of the Seebeck coefficient. Thirdly, the main Seebeck measurement techniques are reviewed and discussed.

Chapter 3 presents the experimental conditions. This encompasses the choice of the materials and samples. Their preparation and processing through growth are detailed. Also, the list of the equipment is provided, along with their settings.

Chapter 4 presents results on the process of growing Ge NWs, with the specific focus of further integration into an oxide matrix using spin-on-glass. The importance of using short NWs, and the subsequent growth parameter adjustments to be made in order to achieve this objective will be explained. Final

integration results are presented and discussed. The fabricated structures are later used for TE characterization.

Chapter 5 presents the results of the TE characterization and analysis, more specifically on the measurement of the Seebeck coefficient. This is followed by a comparison of the experimental results with expected values, and a comparison of devices with each other.

2. Literature Review

2.1 Low-Dimensionality and Thermoelectrics

2.1.1 Early History of Thermoelectrics

From the 1960s to the 1990s, the thermoelectrics field received very little attention from the worldwide scientific research community. In the early 1990s, the US Department of Defense (DoD) became interested in the potential of thermoelectrics for new types of applications. Meanwhile, a resurgence of interest began in the mid 1990s when theoretical predictions suggested that thermoelectric efficiency could be greatly enhanced through nanostructural engineering. Two research approaches were simultanously considered: using new families of advanced bulk thermoelectric materials,[8] [9] [10] and using low-dimensional materials systems [11] [12] [13] [14]. Among the proposed advanced bulk materials, phonon-glass/electron-crystal (PGEC) materials [15] quickly became prominent. As for low-dimensional materials systems, major efforts focused on nanocomposites. These structures containing a coupled assembly of nanoclusters showing short-range low dimensionality embedded in a host material [16] [17] resulting in a bulk material with nanostructures and many interfaces that scatter

phonons more effectively than electrons.

2.1.2 Maximizing the Thermoelectric Figure of Merit ZT

In thermoelectrics, ZT (upper case) is used to distinguish the device figure of merit from the lower-case $zT = \frac{S^2\sigma T}{k}$, the material's figure of merit [18]. To maximize the thermoelectric figure of merit zT of a material for a specific temperature T, a large thermopower S (absolute value of the Seebeck coefficient), high electrical conductivity σ, and low thermal conductivity k are required. As the dimensionality is decreased from 3D crystalline solids to 2D (quantum wells) to 1D (quantum wires) and finally to 0D (quantum dots), new physical phenomena are also introduced and these phenomena may also create new opportunities to vary S, σ, and k more independently than in traditional bulk materials. These parameters, remain, however surprisingly conflicting, as the variation of these parameters can cause an unintended change in another parameter as explained below.

2.1.3 Conflicting Thermoelectric Parameters

Conflict S vs. σ

To ensure that the Seebeck coefficient is large, there should only be a single or dominant type of carrier. Low carrier concentration insulators and even semiconductors have large Seebeck coefficients according to the following equation [19] :

$$S = \frac{8\pi {k_b}^2}{3eh^2} m^* T (\frac{\pi}{3n})^{2/3} \tag{2.1}$$

where,

k_b is the material's thermoconductivity

m^* is the effective mass of the carriers

n is the carrier concentration

e is the elementary charge, $e = 1.60217646 \times 10^{19}\ C$,

h is Planck's constant, $h = 6.626068 \times 10^{-34} m^2 kg s^{-1}$, and

T is the temperature.

However, low carrier concentration means low electrical conductivity, which in turn lowers ZT. Despite this compromise, it was found that good thermoelectric materials are typically heavily doped semiconductors with a carrier concentration between 10^{19} and 10^{21} carriers per cm^3 [20]. Doping effects on ZT are discussed further in Section 2.1.7.

Conflict m^* vs. σ

Equation (2.1) also involves effective mass m^*. Large effective masses produce high thermopower but low electrical conductivity. High mobility and small effective mass are typically found in materials made from elements with small electronegativity differences, whereas large effective masses and low mobilities are found in materials with narrow bands such as ionic compounds. It is not obvious which effective mass is optimum [20]. Indeed no research has yet brought light on the ideal material that would offer the best compromise given the above-mentioned dilemma between high thermopower and high electrical conductivity.

Conflict k_e vs. σ

Thermal conductivity (k) in thermoelectrics comes from two sources:

1. electrons and holes transporting heat (k_e)
2. phonons travelling through the lattice (k_l)

As high zT requires high electrical conductivity but low thermal conductivity, the Wiedemann-Franz law reveals an inherent materials conflict for achieving high thermoelectric efficiency:

$$k_e = LT\sigma k = k_e + k_l \tag{2.2}$$

where L is the Lorentz factor and is a constant[1].

The law decomposes thermal conductivity k as the sum of the electric thermal conductivity k_e and the lattice thermal conductivity k_l. Since k_e is proportional to σ, a high electrical conductivitity conflicts with a low thermal coductivity, which is clearly seen in the following equation , based on Equation (2.2):

$$k = LT\sigma + k_l \tag{2.3}$$

2.1.4 Thermoelectric Improvement Concepts

Concepts aimed at increasing $S^2\sigma$

Low-dimensional thermoelectricity, which is of particular importance for our study, started with the introduction of two concepts: (1) quantum confinement phenomena to enhance S and to control S and σ somewhat independently, and (2) the presence of numerous interfaces to scatter phonons more effectively than electrons, i.e. preferential scattering of those phonons that contribute most strongly to the thermal conductivity. Following numerous proofs of principle, three additional concepts, including carrier-pocket engineering [21] [22] [21], energy filtering [15] [23] and the semimetal-semiconductor transition [24], have further advanced the potential for using low-dimensional materials to enhance thermoelectric performance. The concept of carrier-pocket engineering [25] has been introduced to design a superlattice structure so that one type of carrier is quantum confined in the quantum-well region and another type of carrier of the same sign is quantum confined in the barrier region. The concept of energy filtering [15] [26] [27] of carriers by the introduction of appropriate barriers in the form of interfaces that restrict the energy of carriers entering a material. The concept of semimetal-semiconductor transition occurs during the reduction in diameter of nanowires using a semimetal, such as Bi. The semimetal-semiconductor electronic transition takes place as the lowest conduction sub-band at the L-point

[1] $L = 2.4 \times 10^{-8} J^2 K^{-2} C^{-2}$ for free electrons

moves up in energy, and the highest valence sub-band at the T point moves down in energy. This is how, for instance, Bi nanowires present a semiconducting phase at diameters far below 50 nm, and can be doped to have one-strongly dominant type of carriers. The above mentioned concepts targeted mainly the achievement of a higher value of $S^2\sigma$. Besides and somewhat independently, consistent efforts have been made to reduce the thermal conductivity k.

Concepts aimed at decreasing k

One common feature of the thermoelectrics recently discovered with $zT > 1$ is that most have lattice thermal conductivities that are lower than the present commercial materials.

Three general strategies to reduce lattice thermal conductivity [28]:

1. scattering phonons within the unit cell by creating rattling structures or point defects
2. use of complex crystal structures to separate the electron-crystal from the phonon-glass
3. scattering phonons at interfaces

Increasing $S^2\sigma$ while decreasing k

To increase ZT sufficiently to lead to commercialization of low-dimensional thermoelectric materials, it may not be enough to only decrease the thermal conductivity, but it may also be necessary to increase the power factor $S^2\sigma$ at the same time. It has already been demonstrated that this approach is possible in quantum dot superlattice systems and in nanocomposite thermoelectric materials. The high ZT values achieved in superlattices are to a large degree due to their low thermal conductivity. However, interstingly, it was shown that periodicity is not necessary to reduce thermal conductivity. It is instead important to introduce many interfaces that are specially chosen to:

1. to reduce the thermal conductivity more than the electrical conductivity by interface scattering

2. to increase S (for example, by carrier-energy filtering or by same quantum confinement) more than decreasing the electrical conductivity, thereby yielding an increase in power factor, with both goals helping to increase ZT

k can be reduced by using bulk semiconductors of high atomic weight [3]. S is proportional to the energy derivative of the density of electronic states. In low-dimensional (nanostructured) systems the density of electronic states has sharp peaks [29] [30] [31] and, theoretically, resulting in a high thermopower. Nanostructures may be prepared with one or more dimensions smaller than the mean free path of the phonons and yet larger than that of electrons and holes. This potentially reduces k without decreasing S [32]. Indeed, when a physical dimension is smaller than the mean free path (of electrons or phonons), the particles are limited to this latter dimension, which act like a shorter mean free path. Shorter mean free paths induce less conductivity. This establishes the connection between the mean free path, the physical dimensions, and the effect on the conductivity of either electricity of heat.

2.1.5 Defining the Nanoscale of Thermoelectrics

Mildred *et al.* [28] presented very encouraging results on the possibility of combining the above concepts discussed in Section 2.1.4, using a device based on Si-Ge nanocomposite materials. Thermal conductivity for their nanocomposites can fall below that obtained for their parent bulk samples for cases where the composites contain particle sizes in the 10 nm range for Si_xGe_{1-x} alloy compositions in the range of $0.2 < x < 0.8$. By testing different nanoparticle sizes, they found that for nanostructural widths of 50 nm or less, the mean free path is limited by the nanostructural width d_W, so that the thermal conductivity k now becomes more sensitive to the velocity of sound and specific heat rather than

to the bulk mean free path for scattering. In other words, introducing nanostructured elements of 50 nm and less allows for the device to show behaviour different from that observed in bulk materials. It must be stressed that for the smaller nanostructure sizes in the 10-50 nm range, lowest thermal conductivities are obtained for a high proportion of Si vs. Ge. However as mentioned earlier, the sole consideration of thermal conductivity is not sufficient and a reasonable comparison of Si vs. Ge can only be performed by considering the effect of the Si and Ge ratios on $S^2\sigma$. Not only ordered structures are not necessary to achieve a low thermal conductivity, but it is not required to have coherent interface structures to reduce thermal conductivity [28].

2.1.6 State-of-the-art Thermoelectrics

Nanocomposites

Nanocomposites consist in embedding nanoparticles in a host material to increase its thermoelectric performance. It is possible for a nanocomposite material to increase its power factor and to decrease its thermal conductivity at the same time as shown by Mildred *et al.* Nanoparticles exhibit an energy-filtering effect [33], which strongly lengthens the relaxation time of the phonon scattering. Theoretical analysis of the phonon scattering by a nanoparticle showed that mid- to long-wavelength phonons were scattered more effectively. Nanoparticles also perform an energy-filtering effect that preferentially scatters those phonons that contribute strongly to the thermal conductivity. Because these materials often show best performance for temperatures in the 900K range, long-term stability of the desired nanostructure is required at high temperature and under operating conditions. Also, materials science studies of the effect of porosity on the transport properties show that the electrical conductivity of the nanocomposite changes by orders of magnitude when the sample density changes by only a few percent. Modeling is expected to play a major role in suggesting strategies for the optimization of processes for materials selection, for selection

of the particle-size distribution, and for the design of interfaces to maximize phonon scattering relative to charge-carrier scattering [28].

Trends and challenges in Nanostructure Thermoelectrics

Glasses exhibit some of the lowest lattice thermal conductivities. Good thermoelectrics are therefore crystalline materials that manage to scatter phonons without significantly disrupting the electrical conductivity. Thermoelectrics therefore require a rather unusual material: a 'phonon-glass electron-crystal' [34]. Traditional thermoelectric materials have used site substitution (alloying) with isoelectronic elements to preserve a crystalline electronic structure while creating large mass contrast to disrupt the phonon path. Thermoelectric efficiency could be greatly enhanced by quantum confinement of the electron charge carriers [35] [36]. One common characteristic of nearly all good thermoelectric materials is valence balance - charge balance of the chemical valences of all atoms. The ideal thermoelectric material would have regions of the structure composed of a high-mobility semiconductor that provides the electron-crystal electronic structure, interlaced with a phonon-glass. The phonon-glass region would be ideal for housing dopants and disordered structures without disrupting the carrier mobility in the electron-crystal region [20]. Oxides typically have low mobilities and high lattice thermal conductivity, due to the high electronegativity of oxygen and the strong bonding of light atoms, respectively. These properties give oxides a significant disadvantage as a thermoelectric material. Recent efforts [37] [38] [36] on Bi_2Te_3-Sb_2Te_3 and PbTe-PbSe films and Si nanowires [3] [2] have shown how phonon scattering can reduce lattice thermal conductivity to near k_{min} values [39] [40](0.2-0.5 $W.m^{-1}.K^{-1}$). Thin films containing randomly embedded quantum dots likewise achieve exceptionally low lattice thermal conductivities[41] [42].Very high zT values (>2) have been reported in thin films but the difficulty of measurements makes them a challenge to reproduce in independent laboratories [20]. The challenge for any nanostructured bulk mate-

rial system is electron scattering at interfaces between randomly oriented grains leading to a concurrent reduction of both the electrical and thermal conductivities [43].

2.1.7 Effect of doping on ZT

Bismuth telurride (Bi_2Te_3) was first investigated as a material of great thermoelectric promise in the 1950s [44] [45] [46] [47] [48]. It was quickly realized that alloying with antimony telluride (Sb_2Te_3) and bismuth selenide (Bi_2Se_3) allowed (amongst other goals) for the fine tuning of the carrier concentration. By adjusting the carrier concentration, zT can be optimized to peak at different temperatures, enabling the tuning of the materials for specific applications such as cooling or power generation [49] [50]. Good thermoelectric materials are typically heavily doped semiconductors with a carrier concentration between 10^{19} and 10^{21} carriers per cm^3 [20]. Successful, high-temperature (>900 K) thermoelectric generators have typically used silicon-germanium alloys for both n- and p-type materials [20]. However, in the present study, the silicon sample only serves as a substrate which is needed only to provide a medium of transport for heat and electrical carriers. The objective is therefore not to optimize the thermoelectric properties of the silicon substrate, which could be done by either doping a substrate or by selecting a substrate that is already doped to be in the above-mentioned optimal range of carrier concentrations. It is unclear whether this optimal range of carrier concentrations applies to all nanostructured materials, in particular Ge nanowires (Ge NWs). It is consequently suggested for future research to study the effect of nanowire carrier concentration on the power factor. This point will be stated in the conclusion chapter.

2.2 Towards Semiconductor Nanowires

2.2.1 Recent Research on the Thermoelectrics of Silicon Nanowires

In order to continue the ever impressive and successful improvement pace of thermoelectric devices, tremendous research efforts have been devoted to the search of new materials, combinations or structurations to complement traditional thermoelectric materials such as Bi and Te, which in bulk form have approached their theoretical limits performance-wise. As recent research has proven that Si in the form of nanowires has better thermoelectric properties, one may want to explore whether other semiconductors, somewhat close to silicon, could show better or similar results. Bulk silicon has a ZT of about 0.01 at 300 K (27 °C). For metal wires, the best value at 300 K is about 0.03. Values of 0.7-1.0 are now found in commercially available thermoelectric materials based on bismuth-telluride semiconductors, and its alloys with Sb, Se, and so on. Bulk Si, however, has a high k (150 $W.mK^{-1}$ at room temperature)[51], resulting in ZT < 0.01 at 300 K [52]. The nanoscale geometries of the silicon wires reduce the thermal conductivity by about 100 times. Hochbaum *et al.* [2] quotet a ZT value of 0.6 for their silicon nanowires, while Boukai *et al.* [3] reported a ZT of about 0.4 at 300 K, and around 1 at 200 K. The main advantage of using Si nanowires for thermoelectric applications lies in the large difference in mean free path between electrons and phonons at room temperature: 110 nm for electrons in highly doped samples [53] [54] and, 300 nm for phonons [55]. Consequently, incorporating structures with critical dimensions/spacings below 300 nm in Si should reduce the thermal conductivity without significantly affecting $S^2\sigma$. Hochbaum *et al.* and Vining *et al.* seem to disagree on whether the Seebeck coefficient S is increased in the nanowire form. Hochbaum *et al.* reported electrochemical synthesis of large-area, wafer-scale arrays of rough Si nanowires that are 20-300 nm in diameter. *These nanowires have Seebeck coefficient and electrical resistivity values that are the same as doped bulk Si, but those with diameters of about*

50 nm exhibit 100-fold reduction in thermal conductivity, yielding ZT = 0.6 at room temperature [2]. Contrastingly, according to Vining *et al. the smaller size reduces the electrical conductivity of the rectangular nanowires, partly negating the benefit of their decreased thermal conductivity. Second, and more importantly (as the Seebeck coefficient is squared in the expression for the figure of merit), it (the smaller size) greatly increases their Seebeck coefficient* [56]. Vining belives that the phonon drag is responsible for the larger Seebeck coefficient, larger thermal voltages and higher efficiency. It has been shown that the k of Si nanowires (grown by vapour-liquid-solid process) is strongly diameter-dependent [57] of , which is attributed to boundary scattering of phonons [2]. As an important proof of concept has been achieved regarding nanowire devices using simple materials, further research may find out what other materials might show the effects of low thermal conductivity and large phonon drag.

2.2.2 Why Germanium may be interesting

Germanium is an important semiconductor with a direct bandgap of 0.8 eV and an indirect bandgap of 0.66 eV. Recently, interest in germanium has intensified as the migration from silicon to other materials is contemplated for enhanced functionality of future transistors for logic and other functions. Compared to bulk silicon, bulk germanium offers several advantages:

- Higher intrinsic carrier mobilities ($\mu_n = 3900cm^2.V^{-1}.s^{-1}$ and $\mu_p = 1900cm^2.V^{-1}.s^{-1}$ for Ge versus $\mu_n = 1500cm^2V^{-1}s^{-1}$ and $\mu_p = 450cm^2.V^{-1}.s^{-1}$ for Si at 300 K) [58] [59]
- Higher intrinsic carrier concentrations ($2.4 \times 10^{13}cm^3$ for Ge versus $1.45 \times 10^{10}cm^3$ for Si)
- Larger bulk excitonic Bohr radii (24.3 nm for Ge versus 4.7 nm for Si)
- More prominent quantum-confinement effects [60] for bandgap control of the nanostructures

- Compatibility with high-dielectric-constant materials, [61] enabling integration with current semiconductor processing technology

Considering both the recent exciting research results on Si NWs and the above-mentioned potential ZT-relevant advantages of Ge over Si, it becomes interesting to explore devices based on Ge NWs.

2.3 Germanium Nanowires Growth Mechanisms

2.3.1 Vapour-Liquid-Solid growth mechanism

In 1964, to explain the growth of single crystal silicon wires, Ellis and Wagner introduced the vapour-liquid-solid growth mechanism (VLS) [62]. They explained that the mechanism involves typically three phases: vapour precursor, liquid alloy, and solid wire. Since, a plethora of studies have mentioned the VLS mechanism to explain the growth mechanism of various types of NWs. An important characteristic of the VLS growth mechanism is the use of a metal catalyst to seed the growth. The stability and low eutectic temperature of the Au-Ge alloy make it an ideal and widely used catalyst for the growth of Ge NWs. Based on Ge NWs that were grown using a CVD method, Sun *et al.* [63] illustrate the three simultaneous processes involved in the VLS mechanism.

Alloying

A vapour precursor containing germanium is flowed into a low-pressure chamber containing a sample covered with catalyst seeds. The molecular or atomic nature leads to a nuance in the creation of the alloy. On the one hand, when the precursor is a molecule embedding the semiconductor of interest, which is the case for CVD methods involving germane GeH_4 or digermane Ge_2H_6, physisorption of the precursor on the metal seeds occurs. The bond then breaks and releases free germanium atoms that incorporate into the metal catalyst. On the other hand, when the precursor is germanium vapour, which is common in vapour transport methods, germanium atoms are directly absorbed into the metal seed. In both cases, incorporation of pure germanium into the gold catalyst occurs and forms a binary alloy. At this stage, the alloy is in a liquid state since the growth temperature (or sample temperature) is typically above the eutectic temperature of the alloy (361°C for Au-Ge).

Nucleation

In the early stage of alloying, the Ge concentration in the alloy is low and increases with the incorporation of incoming Ge atoms. Ultimately the alloy reaches supersaturation, a phenomenon that occurs when at least one of alloy components reaches the maximum allowable percentage for the sole liquid state to exist at a given temperature. After supersaturation has begun, nucleation occurs when the alloy enters a dual phase region characterized by the presence of Au-Ge liquid alloy and Ge solid crystal.

Axial Growth

When nucleation begins, there is a preference for accumulation of the solid crystalline germanium at the alloy-substrate interface. This peculiar phenomenon is attributed to energy matters. Through accumulation at the alloy/substrate interface, the event of crystal growth minimizes the energy of the supersaturated alloy as compared with continuous nucleation within the alloy [64]. When crystallization has begun, further incorporation of germanium into the alloy increases the amount of Ge crystal precipitating out from the alloy. As a consequence of Ge crystal accumulation underneath the alloy, the liquid-solid interface between the alloy and the crystal is then "pushed" upwards and enables a crystalline to wire grow underneath the alloy tip. When the chamber cools down, the alloy tip solidifies. These catalytic tips, frequently observed under SEM and TEM, are commonly used as the evidence that the growth followed the VLS mechanism.

2.3.2 Vapour-Solid-Solid growth mechanism

Most of the nanowire syntheses are performed at a temperature higher than the eutectic temperature. However, some studies that reported Ge NWs growth eutectic temperature generated debate on the solid or liquid nature of the catalytic tip. Using real-time in-situ microscopy, Kodambaka *et al.* [65] succeeded in resolving this issue. They discovered that liquid or solid particles can induce

growth. According to the authors, whether a wire grows via a solid or liquid particle is dependent on growth pressure, thermal history, and NW diameter. Following the growth phase, the growth mechanism that generated the NWs can be identified by observing the shape of the NW tip. While VLS-grown NWs are characterized by a spherical shape, VSS-grown wires presents flat surfaces, sharp edges and generally speaking cubic shapes.

2.4 Germanium Nanowires Growth Methods

The most common methods to synthesize germanium nanowires (Ge NWs) are essentially Chemical Vapour Deposition (CVD) [66] [67] and vapour transport [68]. Various other methods exist, including laser-ablation, solution synthesis, electrochemical etching [69] and oxidation-based thinning down of lithography-patterned NWs. These alternatives will not be discussed here either as they are not relevant for the NW growth method used in this project. Growth using CVD methods commonly follows the same growth mechanism, known as Vapour-Liquid-Solid (VLS) growth, for the synthesis of Ge NWs. Most differences between synthesis methods lie in the production of the vapour of the reactants, which contains the semiconductor atoms of interest. Using a CVD method to grow single-crystalline Ge NWs means typically using germane GeH_4 or digermane Ge_2H_6 gas. In other methods than CVD, reactant vapour is generated either by thermal evaporation or by directing laser pulses on solid targets of the given semiconductor. In the following, our interest will focus exclusively on CVD and vapour transport.

2.4.1 CVD

Chemical Vapour Deposition (CVD) allows for the synthesis of single crystalline Ge NW at relatively low temperatures, by flowing germane GeH_4 into a low-pressure chamber containing a sample covered with (most commonly but not

only – see Section 2.4.3) Au nanoseeds. It is widely accepted that this growth method follows the Vapour-Liquid-Solid (VLS) mechanism decribed in Section 2.3.1. Germane GeH_4 decomposes to give Ge, which forms a binary alloy with the Au seeds. By supersaturation, excess Ge crystallizes under the alloy to form a single crystalline NW. Critical parameters, such as length and diameter, are determined predominantly by the growth duration and size of the nanoseeds, respectively. Since GeH_4 decomposes easily, and the Ge-Au binary alloy has a low eutectic temperature, growth temperatures as low as 275°C can be used. The key to an optimum growth is to find the good balance in terms of Ge feeding and Ge diffusion in the seeds. Understanding and refining the growth chemistry enable excellent control over the synthesis. For example, 100% yield of Ge NWs relative to the Au seeds can be obtained, with one-to-one correspondence of NWs to the seeds [70]. This result leads to deterministic Ge NW synthesis by patterning of individual Au nanoclusters. Furthermore, these deterministically grown NWs can be aligned into quasi-parallel arrays with a simple post-growth fluidic treatment [70]. Additionally, in situ doping during the growth is achieved with co-flows of precursors containing desired dopants, e.g. PH_3 for n-type and B_2H_6 for p-type, and the doping level can be controlled by adjusting the ratio of Ge to dopants.

2.4.2 Vapour Transport

In contrast with CVD methods, in which growth results from a chemical reaction between a gas and a catalyst, vapour transport involves physical vapour deposition. The process presented in the following is generic to most studies reporting vapour transport growth. A small quantity of highly purified Ge powder is put in a ceramic crubible, sometimes along with another material used as a carrier. This crucible is placed in the sealed end of a quartz tube. Further away in the tube are placed the samples on which it is intended to grow Ge NWs. The location of the crucible and of the samples are meant to match respectivily the high-

temperature and low-temperature zones of the horizontal furnace tube in which the quartz tube is placed. The furnace tube is generally made of alumina, so as to withstand very high temperatures, ranging around 1000°C, that are needed to evaporate the germanium powder. The later tube is then sealed and evacuated. The pressure is generally controlled, as well as the flow of an inert gas such as argon. Some studies reported the use of an additional gas that plays a role in improving the growth conditions. Wu and Yang [71] reported in 2000 that prior to their study, the growth of Ge NWs had been sparsely documented. They present a process in which they use a mix of 30 mg Ge powder with 7 mg GeI_4 to grow Ge NWs on Si (001) coated with 50-200 Å thick gold thin films. The crucible was heated to 1000-1100°C with a gradient of temperature of 100-200°C between the crucible and the samples, which represents a relatively high sample temperature as compared to other studies. After 30 minutes of vapour transport, the chamber was air cooled. The resulting NWs were hundreds of nanometers long and their diameters ranged between 5 and 300 nanometers. Interestingly, they realised that thinner Au films allowed the control of the NWs' diameter; 100 Å would yield an average diameter of 150 nm, while 50 Å would bring it down to 80 nm. It was reported that lower Au thicknesses did not result in thinner wires. To address this limitation, they proposed an unconventional method for further thinning down of the wires by reheating them. The purity and crystallinity of the initial nanowires were examined using X-ray diffraction (XRD). The diffraction peaks confirm the diamond structure of germanium, although a residual amount of I_2 was detected. A TEM examination confirms that the VLS method growth method occured as well as showing that the wires are grown predominantly along the [111] direction.

Nguyen *et al.* [68] brought more insight to the vapour transport method. Their source was composed of an 1:1 weight ratio of germanium nanopowder and synthetic graphite powder. The graphite is insoluble in crystalline germanium at the considered temperatures. It is essentially used to increase the surface

area for the evaporation of germanium, to control the germanium partial pressure, and to reduce the amount of germanium oxide by carbothermal reduction. They achievied successful growth of Ge NWs organized matrices on Ge samples. It was achieved with gold catalyst dots of 100 nm diameter and 5 Å thick after incremental changes of the catalyst size and thickness. The fabrication of catalyst dot arrays used sequentially e-beam lithography, ion-beam sputtering-gold deposition and resist lift-off. The average diameter of the Ge NWs was 38 nm. It must be stressed that the sidewalls of nanowires were found to be particularly smooth, which is not necessarily interesting for thermoelectric applications. It is believed that rough surfaces provide more of the desired phonon scattering to decrease the thermal conductivity. A variety of substrates were explored, including silicon carbide, highly doped (111) silicon and different planes of crystalline sapphire. The resulting non-vertical growth were due to lattice mismatch, above 25% in all cases, except for silicon (4% only) which shows a large proportion of almost vertical wires. It is therefore infered that an atomic buffer layer of germanium deposited on silicon (111) would provide lattice-strain relaxation and is thus very likely to yield vertical Ge NWs. Uniform vertical NWs are achieved in this study with a source temperature of 1020-1030°C, a substrate temperature of 470-480°C, and a carrier gas of 100-140 sccm argon and 50-80 sccm hydrogen. Hydrogen is used to minimize oxidation while providing a passivation layer.

Sun *et al.* [72] provided more insight on electronic and local structures of GE NWs grown using the vapour transport process. In many aspects, the growth conditions they report are similar to other studies, yet with a few interesting recommendations and variants. Germanium of high purity was used as the sole precursor. The temperatures of the crucible and of the silcon or alumina sample were respectively 950°C and about 600°C. Argon was used as the sole carrier gas, flowing at 50 sccm and 200 Torr. They synthetised thiol-caped gold nanoparticles [73] that are on average 2 nm in diameter. It resulted in an average nanowire diameter of 30 nm. The study confirms that the Ge NWs did not match

the size of the Au particle. It is seemingly due to aggregation of gold particles at high temperatures. The above-mentioned temperatures were established at a ramp of 15°C per minute then it is maintained at the desired temperature for 1 hour. It can be assumed that the post-growth temperature decrease followed a simple exponential cooling curve as it is often the case in thermal systems that are allowed to cool down naturally with no artificial cooling system. The resulting length of Ge NWs is tens of micrometres. Structurally, the nanowires are single crystal with a diamond structure and predominantly in the <111> direction.

Through these studies, many advantages of the vapour transport process are commonly highlighted. The advantages compared to other methods include simple reactor setup, minimal equipment investment and use of non-hazardous materials and gases. This literature survey on vapour transport processes suggests high correlations between certain growth parameters and critical aspects, such as nanowire diameter, length and preferred growth directions. This is addressed in the following section.

2.4.3 Growth parameters

Catalyst Material and Size

The synthesis of VLS- or VSS-grown self-assembled NWs nanowires requires a metal seed, which serves as the seed for NW growth. The metal catalyst is instrumental in defining critical parameters of the resulting NWs; their location, diameter and crystal orientation. A non-exhaustive list presents advantages and drawbacks of several catalysts that were encountered in the literature. This list includes Au, Fe, Al, Ni, In, Sb and concludes with studies reporting catalyst-free VLS growth.

Au catalyst Due to its ability to form alloys with Ge or Si with low eutectic temperature, Au remains to date the most prominent and frequently used metal

catalyst. The eutectic temperatures for the Au-Ge and Au-Si alloys are respectively 361°C and 363°C. Low values of eutectic temperatures are desirable as they enable the use of low growth temperatures. The lower the eutectic temperature, the higher the probability of reactants to incorporate onto the catalyst and typically, not on the substrate or on the NW's body. Along with the appropriate growth conditions, the choice of a low eutectic temperature is critical to the achievement of excellent uniformity in the diameter of NWs. An unwanted side effect of Au used as a NW catalyst is the formation of deep electron traps, which makes Au an unsuitable catalyst for CMOS applications. No published study was found to relate this drawback to TE performance, or less directly, on the electrical conductivity.

Fe catalyst Lieber *et al.* reported Fe-seeded growth of Si and Ge NWs using the laser ablation method [74]. Fe-Si and Fe-Ge alloys have very high eutectic temperatures, 1207°C and 838°C respectively. For the VLS mechanism to happen, the use of Fe requires high growth temperatures. The authors mentioned for instance that Si NWs form at temperatures above 1150°C, and 820°C for Ge NWs.

Ni catalyst Nickel, which is a CMOS-compatible metal, has been reported to successfully catalyze the growth of Ge NWs. [75]. Nickel-seeded Ge NWs are synthetized in supercritical toluene at 410°C, which is 352°C below the eutectic temperature of Ni-Ge. The growth mechanism is however not VLS but SLS, which denotes the Solution-Liquid-Solid mechanism. The SLS mechanism involves complex methods and specific equipement. It is mentioned here only for general information purpose.

Al catalyst Aluminum is another suitable CMOS-compatible catalyst for Ge NW growth [76]. Al is readily available and widely used in CMOS processes. Its alloys with Si and Ge have encouragingly low eutectic temperatures, which

enable the synthesis of Al-seeded Si NWs at 465°C [76] using a CVD method.

In and Sb catalysts Lately, indium (In) and antimony (Sb) were also reported as possible catalysts to produce Ge NWs [77]. The eutectic temperatures of the In-Ge and Sb-Ge are relatively low. More interestingly, what makes In and Sb is their ability to be used as dopants, as is the case in front-end processes for doping [78] [79] in transistors. Used as solid dopant sources that would be evaporated, highly purified In and Sb could offer an interesting alternative to the highly-toxic gas-phase diborane (B_2H_6) and phosphine (PH_3) used in CVD processes. Applied to vapour-transport, which uses Ge powder instead of the toxic digermane, In and Sb doping would form an interesting low-risk and simple alternative to the toxic and more complex CVD of germane/diborane or germane/phosphine. The dopant profile along the nanowire can be extracted by scanning capacitance microscopy.

Catalyst-free methods While intense works are being carried out to search for alternative metal catalyst seeds, researchers are also exploring NW growth without the use of catalysts. Zaitseva and co-workers have demonstrated that unseeded growth of single-crystal Ge NWs is possible [80]. In their experiment, tetraethylgermane (TEGe) was used as the precursor and the supercritical growth was carried out in a reactor with different solvents.

Catalyst Size

The range of catalyst sizes that can yield NW growth is in fact fairly narrow. The VLS mechanism is such that the catalyst size determines the diameter of the nanowire [66]. Successful Ge NW growth with large catalyst sizes (above 50 nm) was reported using CVD methods [81] but the technique already involves peculiar constraints such as the growth of multiple NWs per large gold seed. More focus should be placed on the lower limit as both Moore's law and thermoelectrics recent findings encourage scaling down the nanostructures of in-

terest. In the particular case of thermoelectrics, the objective is to reduce the mean free path of the phonons. This is achieved by reducing the dimensions of the nanstructures of interest, in our case Ge NWs. The process of improving NW-based thermoelectrics therefore involves exploring the lower limit on the NW diameter. The mean free path of electrons remains superior to the smallest dimension as established in Section 2.1.4, otherwise it may lower the electrical conductivity, which in turn reduces the figure of merit. Therefore the choice of the ideal catalyst size must ensure that the subsequent NW diameter will be above this limit. Additionally, it was also previously mentioned that smaller diameter give better thermal conductivities. As a consequence, the catalyst size may also ensure a diameter as close as possible to the limit beyond which further gain in thermal conductivity results in a loss on electrical conductivity. In simpler terms, the ideal diameter is somewhere right above the mean free path of electrons. If for this diameter the wire cannot exist, then the best value will by default be the lower diameter limit that permits growth.

The minimum catalyst diameter at which VLS growth of Ge NWs can occur can be explained by the Gibbs-Thomson equation [82]:

$$\frac{\Delta\mu - \Delta\mu_0}{kT} = \frac{4\Omega\alpha_{vs}}{kT}\frac{1}{d} \tag{2.4}$$

where,

$\Delta\mu$ is the effective difference between the chemical potentials of Ge in the vapour phase or liquid phase and in the nanowire,

$\Delta\mu_0$ is the effective difference between the chemical potentials of Ge in the vapour phase and a planar interface,

Ω is the atomic volume of Ge,

d is diameter of the nanowire, and

α_{vs} is the the specific free energy of the nanowire surface.

In Equation (2.4), a simple extreme case consideration illustrates that if the

diameter d decreases, the difference $\Delta\mu - \Delta\mu_0$ has to increase. Since $\Delta\mu$ is a constant, the difference is maximized by cancelling $\Delta\mu_0$, which represents the supersaturation potential. In other terms, the critical diameter corresponds to the absence of supersaturation, which is indispensable for nucleation and axial growth to take place. The critical diameter d_c representing the lower diameter limit is thus given by the following equation:

$$d_c = \frac{4\Omega\alpha_{vs}}{\Delta\mu_0} \tag{2.5}$$

Seed Density

Not only are the Ge NWs characteristics dependent on the catalyst size but density also plays a major role. As demonstrated by Bakkers *et al.*, the wire lengths increase with decreasing wire-to-wire spacing L, for constant catalyst size [83]. They also observed that the wire length increase is highly correlated with NW diameter. The possible cases are classified into 3 regimes, each of which exhibits different growth rates and behaviours with respect to catalyst size and spacing.

High Density – Catalyst Spacing below 0.7μm In this scenario, the NWs compete for precursor. Due to faster supersaturation, thin NWs were found to grow faster than the thicker NWs. It is indeed trivial that smaller catalysts require less precursor to reach supersaturation. If the density is decreased, there is not as much need for competition, given the lower overlapping of surface collection areas for each NW. Therefore, for this regime characterized by $L \leq 0.7\mu m$, the growth rate increases accordingly with spacing. This regime was refered to as "the material competition regime".

Low Density – Catalyst Spacing above 3μm The above-mentioned regime suggests that it is the overlapping surface collection areas of the nanowire that create competition. Above a certain minimum seed spacing, these surfaces do not overlap any longer. This phenomenon is indeed observed with low seed

densities ($L \geq 3\mu m$). In such a configuration, there is no apparent interaction nor competition between neighbouring NWs. Because an increase of spacing does not reduce competition, no increase in growth rate is observed. Each wire can thus be considered as independent from the rest. This regime was refered to as "the independent regime".

Intermediate Density – Catalyst Spacing $\mathbf{0.7\mu m \leq L \leq 3\mu m}$ In this odd regime, where the NWs are yet subject to competition, the growth rate is found to increase as the dots are more dense. These unexpected diameter- and spacing-dependent growth rates are a result of the synergistic growth of the NWs. Once the material competition regime is exceeded, the growth rate becomes dependent on the surface fraction of the seeds. Denser spacing means a larger surface fraction and results in a faster growth rate.

Methods of Catalyst Deposition

The size of the catalytic seeds determines the diameter of the NWs and also affects the growth rate. Similarly, the positions of the seeds define precisely where the NWs will originate. The deposition of the metal catalyst is therefore a very crucial step for NW assembly and applications, especially for devices with complex patterns which require precise spatial control of the NWs. There are several methods used to deposit the metal catalyst, each with their drawbacks and advantages.

Lithography The required small dimension (tens of nanometers) of the catalyst seed shrinks the pool of lithography candidate methods to electron beam (e-beam) [84] and interference lithography (IL) [85]. E-beam lithography offers the advantage of extreme precision (few nanometers) which allows to design nearly any pattern, with high fidelity and high control over their location and size. The disadvantage of e-beam lithography is the low-throughput of the process. IL is a good alternative with higher throughtput and larger exposure areas.

The spectrum of patterns is however limited to regularly spaced and aligned designs due to the use of light interferences. Both solutions call for particular caution to be exercised regarding the elimination of residual resist so as to avoid contamination in the growth process.

AAO and PS as hard masks In order to deposit regular arrays of catalyst, hard masks, such as anodized aluminum oxide (AAO) [86] or polystyrene spheres (PS) [87], can be used. Control over the pores size of the AAO membrane is permitted by adjusting anodization conditions and electrolytes. The size of the pores is that of the subsequent desired catalyst seed. In the same fashion, the size of the polystyrene spheres determines the size of the evaporated or sputtered shapes. Analogously with electron-beam lithography (EBL) and IL, the use of AAO or PS to deposit metal catalysts can cause contamination during the transfer or removal of the AAO, or the mono-dispersion of PS. It must also be mentioned that these methods require a high level of patience and carefulness that make the process very slow and tedious.

Thin film deposition followed by annealing To address the recurring problems of contamination and complexity, thin metal films, such as Au, can be first deposited on a clean substrate, typically in a high-vacuum evaporator chamber. The thin film is then annealed, which forms self-assembled individual metal dots. The size of the subsequent metal seeds follows a gaussian distribution. Given the dependence between seed size and nanowire diameter, the diameter of NWs follows a similar distribution. There are several cases in which a large variance of this distribution is undesirable. In low-scale electronics, such as NW transistor design for instance, it is important to use NWs with precise dimensional criteria. It is also undesirable in thermoelectrics if a significant portion of NWs has a large diameter above the size threshold which gives better performance. The formation of self-assembled islands is temperature-, pressure- and material-dependent. For instance, on silicon substrates, gold is widely used be-

cause it yields metal seeds very easily, while titanium (Ti) will form $TiSi_2$ with the silicon substrate and may not agglomerate to form self-assembled individual islands.

Although imperfect, the annealed thin film method is one of the most frequently used methods because simplicity and low-contamination risk. It is sufficient for applications or studies where the precise diameter of the NWs is not a critical factor.

Colloidal solutions Colloidal solutions offer a particularly simple way to deposit metal seeds for NW growth. The metal nanoparticles come in a solution and their size can be as small as a few nanometres. They can be simply deposited or evenly spun onto the substrate. This can be followed by an annealing step to enhance adhesion and partially evaporate the solvent. Au colloidal solution is a popular choice for NW growth. Because Au particles do not adhere well on Si samples, the Au deposition is often preceded by the application of a monolayer of AminoPropyl TrimethoxySilane (APTS). The density of gold colloids can be controlled by the pausing time after simply putting a drop on the sample and prior to blow-dry the solution. The colloid method also suffers from issues of contamination and is criticized for presenting a very low ratio of grown NWs versus available seeds.

Temperature

Temperature and Morphology It was established earlier that two types of growth are involved with NWs; these are namely axial and radial growth. Axial growth occurs at the liquid-solid interface between the metal alloy and the crystalline NW. As it pushes the wire to grow upwards, the wire becomes vertically longer. Radial growth however makes the wire thicker. It results from the bonding of precursor on the sidewalls of the NWs. Although these two processes take place independently, temperature is the key factor that influences each of the mechanisms. The focus here will be specifically on radial growth. Like often in the case

of Ge nanowire growth, most of the studies on the influence of various factors are carried out using a CVD system. The reason for this is that CVD systems, much unlike conventional furnaces, offer great accuracy and control of parameters, such as partial pressure of the precursor and more importantly substrate temperature. In conventional multi-zone furnaces, which uses a resistive heating mechanism, the feedback of the temperature control system originates from a thermocouple which measures the resistive coil temperature. It is therefore not reasonable to believe that the sample, inside a quartz tube which is inside the furnace alumina tube, is at the same temperature as that indicated by the thermocouple. In other words, conventional furnaces offer poor control and precision on the growth (or sample) temperature. For CVD systems and using Au seeds, it has been reported by several groups that 300/350°C seems to be the threshold temperature above which tapering starts to take place. Smooth NWs with constant diameters along the NW can be produced through CVD processes at low growth teperature below 300°C [88]. At higher temperatures (above 300°C), the event of radial growth leads to tapering, an effect that is often undesirable on the morphology of the NWs synthesized as it gives them a cone-like shape instead of a uniform diameter along the NW. On the surface of the substrate, it is common at these temperatures to observe direct thin film deposition, the thickness of which also increases with temperature [66] [89] [90]. When the temperature is further increased from 400°C to 600°C, the morphology of the synthesized NWs is changed. Taraci *et al.* reported shifts from tapered NW, to wire-like nanopillars to nano-blocks. Kamins *et al.* supported this finding by reporting "blocky structures" obtained at the temperature of 380°C while good NW morphology was obtained for temperatures between 300 and 350°C. They found that the axial growth rate is proportional to the temperature and can be attributed to the catalytic decomposition of GeH_4 at the surface of the eutectic liquid, which is thermally activated.

Temperature and Catalyst size We observed previously that the diameter of the NWs is strongly determined by the metal catalyst seed size. In fact, the optimal growth temperature also depends greatly on the size to be achieved. Wang *et al.* have lead a study on the effect of temperature on the CVD growth of NWs using different catalyst seed sizes, ranging from 5 to 50 nm [81]. Unfortunately, to date, no similar study involving vapour transport was found in the literature. For each catalyst size, Wang *et al.* found the optimum growth temperature. This optimal temperature was found to increase with catalyst size, in a nearly-linear manner. It must be understood that smaller catalysts can lead to growth at lower temperature, while larger catalysts require higher temperatures. For any given catalyst size, applying a temperature below the optimum will decrease the yield as a sub-optimal number of seeds will nucleate. Applying higher temperatures than the optimal temperature results in the growth of multiple nanowires on single seeds. Understanding the atomic diffusion process is fundamental to explain this nearly-linear relationship between optimum growth temperature and catalyst size. The size of the catalyst seed is the distance through which germanium must diffuse so that it saturates the alloy, thus permitting for nucleation and growth of the wire at the catalytic tip. As a consequence, larger seeds need a higher temperature so that diffision can occur at a comparable pace at that observed at a lower temperature with smaller seeds. It seems the diffusion time in the alloy somewhat has to be constant to synthesize NWs with a similar good form.

Partial Pressure It is widely accepted that higher temperatures increase radial growth whereas higher partial pressure promotes axial growth and eliminates tapering [66] [88] [90]. Several groups have demonstrated a 5-fold increase in axial growth rate when partial pressure is changed form 10 to 50 Torr [91] [66]. This suggests that that the axial growth rate is highly dependant on partial pressure. This can be explained by the VLS growth mechanism. In the VLS process, using a CVD method, the factor that limits the growth rate is assumed to be the

integration rate of the precursor reactant in the liquid catalytic alloy. This rate linearly increases with partial pressure of the precursor. As for the undesirable radial growth, it is minimized by the passivating effect of hydrogen, a by-factor of the decomposition of SiH_4 and GeH_4 [92]. In applications where tapering and radial growth are desirable, which might the case in thermoelectrics to obtain rough surfaces, it must be noted that hydrogen is the rate-limiting factor for radial growth [93]. Further increase of precursor partial pressure in CVD methods increases the amount of surface hydrogen, which, to a certain degree, limits the growth rate in the radial direction. The resulting NWs are found to be straight with very little tapering.

2.5 Integration of Nanowires

Integration consists in embedding the matrix of bare nanowires within a solid material. It must provide the resulting device with the following properties:

- the embeding material must enable the application of pressure on top of the device without damaging the nanowires
- damage caused to the nanowire structure by a probe tip should be minimal
- it must allow the deposition of a conductive layer on top of it to allow probing
- it must resist the subsequent high-temperature processes in the fabrication of the device
- it should prevent electrical carriers from being drawn out of the nanowires
- its thermal conductivity should be as low as possible (to *force* heat transport to occur in the NWs, thus generating a Seebeck voltage)

At least two types of materials are eligible candidates to meet the above-mentioned requirements: dielectrics and polymers. Our interest goes primarily

for dielectrics mainly because standard polymers are only thermally stable up to about 275°C. Using polymers would limit the device's temperature range of use. It is indeed expected for Ge based materials to show better thermoelectric properties at higher temperatures. In all cases, the device is meant to undergo measurements from low to high temperatures, which explains why its constitutents must withstand high temperatures, since low temperatures are usually not a problem. Polymers do not allow repeatable high-temperature measurements due to their low range of temperature stability. The polymer's instability at high temperatures also poses a problem of compatibility with further high-temperature processes. It could be interesting indeed to investigate the properties of multiple layers of embedded nanowires. Besides, regardless of the temperature issue, due to poor thermal characterization of polymers by manufacturers, it is not clear whether the thermal conductivity of the polymer is compatible for thermoelectric applications. In view of the above, dielectrics are preferred. Table 2.1 presents a list of high-κ dielectrics[2] commonly used in nanofabrifaction and their respective thermal conductivities.

Our interest being in low thermal conductivities, silicon oxide is undoubtedly prefered in this regard. Silicon oxide integration is potentially achievable using two possible methods, through physical vapour deposition (PVD) or spin-on-glass (SOG). Latu-Romain *et al.* [94] demonstrated successful integration of Ge NWs using these two methods. Other ways of integrating NWs can be explored [95] [96]. Spin-on-glass (SOG) is a mixture of SiO_2 and dopants (either boron or phosphorous) that is suspended in a solvent solution. It is applied and spinned on a silicon sample just like photoresist. After spinning, the SOG has to be cured so that polymerization can occur. The nearer the curing temperature is to room temperature, the better, but the efficiency-concerned researcher may leave his samples in a clean oven at 60°C for 48 hours. At room temperature, a week is generally good enough. While exploring whether the thermal

[2] κ denotes the dielectric constant of the material, not to be mistaken with k which represents the thermal conductivity.

Table 2.1: Popular high-κ dielectrics and their bulk thermal conductivity

Name	Formula	Temp. (°C)	Thermoconductivity $(W.m^{-1}.K^{-1})$
Zirconium Oxide (plasma sprayed)	ZrO_2	20 to 80	0.8
Silicon Dioxide	SiO_2	200	1.05
		400	1.26
		800	1.67
		1200	2.09
		1600	2.51
Hafnium Dioxide	HfO_3	20 to 475	11.43
Yttrium Oxide	Y_2O_3	20	17
Aluminum Oxide	Al_2O_3	20	25.12
		100	16.75
		200	12.56
		315	15.49
		400	8.37
		500	14.66
		600	8.79
		800	6.28
		1000	5.86
		1200	5.44
		1400	5.44
		1600	5.86
		1800	7.12
Aluminum Oxide (Single Crystal)	Al_2O_3	20	43.13
		300	19.68
		800	12.14

behaviour of dielectrics changes with film thickness, it was found that below approximately 250 nm thickness, the observed thermal conductivity of the SiO_2 thin films systematically decreases as a function of film thickness [97]. This agrees with the theory that suggests that whenever a structure's dimension is lower than the mean free path of phonons, the thermal conductivity decreases (see Section 2.1.4). And indeed, the range of roughly [50-300] nm seems to reflect the threshold below which the mean free path of phonons is lower than that found in most bulk materials. For the present study however, since the quest regards a dielectrics of low thermal conductivity, the decrease caused in thin films is all the better.

2.6 Resistivity Measurement

One of the key parameters that play a role in the performance of a thermoelectric device is its conductivity σ, or equivalently, its resisivity ρ. These are linked by the expression $\rho = \frac{1}{\sigma}$. The measurement process of resistivity in thermoelectrics is more complex due to the active nature of the devices. It will be described further in this section. Prior to this, a set of particular warnings should be addressed. Many factors can induce large errors that would be detrimental to an accurate estimation of the thermoelectric figure of merit. Care should therefore be taken in following a certain number of recommended guidelines.

It is tremendously important to calculate ZT using measured values from the same samples. A common mistake is to overtrust the homogeneity of samples coming from the same ingot. It often results in a wrong ZT values that are not realistic as they relate to none of the existing samples taken alone. It is therefore best to make, on the same sample, all measurements of the parameters used in calculating ZT. Additionally, the measurements should be taken together as closely in time as possible so as to minimize the effects of sample detoriation.

There can be a strong dependence of thermal transport properties and electrical properties on crystal orientation. It can go as high as orders of magnitude. Thus, it is important to check the crystallographic direction of the sample of which the measurements are reported.

As for contact effects, it is not uncommon to observe Joule heating (I^2R_c) at electrical contacts between the probe and the sample. This can make the thermoelectric measurements even more difficult as it may cancel the desirable heat gradient.

Often, and particularly in the present study, the devices all rely on silicon samples. In the process of performing electrical measurements, the application of conductive probes onto the sample introduces a metal-semiconductor interface. In order to avoid the problems that can exist in making a good electrical

contact between metals and semiconductors, it is advised to sputter or evaporate a thin layer of about 100 nm or more of gold onto all electrically connected surfaces of the silicon samples.

As resistivity is a key value in the calculation of ZT, the sample dimensions must be known precisely as they are used for resistivity calculation: $\rho = (V/I) \times (A/L_0)$, where ρ is the resistivity, V is the voltage, I the current, A is the surface area of the sample, and L_0 is its thickness.

It is also recommended to use a precision resistor (0.01 to 0.1%) in series within the measurement circuit so as to determine the current with precision. In this study however, in absence of any unreliable external current generator, the current values provided by the parameter analyser shall be sufficient.

As mentioned previously, provided that these recommendations are duly taken into account, the resistivity measurements can be carried out. The protocol is generic and particular to all thermoelelectric devices.

In the presence of a temperature gradient, the apparent measured voltage V_{TOT} is the sum of the Seebeck voltage, $V_{TE} = \alpha\Delta T$, plus the resistive voltage V_{IR}:

$$V_{TOT} = V_{IR} + \alpha\Delta T \tag{2.6}$$

Unlike in passive resistive devices, the Seebeck voltage depends uniquely on the thermal polarity, or in other words the orientation of the thermal gradient. Thus, since the thermal gradient remains the same throughout the measurement, changing the current polarity will not affect the sign or orientation of the Seebeck voltage. As a consequence, by switching current polarity, it becomes then possible to subtract out the Seebeck voltage using the following equation:

$$V_{IR} = \frac{[V_{IR}(I^+) + \alpha\Delta T] - [V_{IR}(I^-) + \alpha\Delta T]}{2} \tag{2.7}$$

where $V_{IR}(I^+) = -V_{IR}(I^-) = V_{IR}$.

The first measurement is done for a negative value of the current, followed by a second measurement performed at the opposite polarity. The period of the signal will be ranging between 2 to 3 seconds in order to minimize the effects of the induced thermal gradient (longer time constant). Particular attention must be paid while thermally anchoring the sample to the heat sink and the thermocouple ends to the sample. The thermocouple ends should be electrically insulated and ideally as close as possible to the voltage contacts.

2.7 Seebeck Coefficient Measurement

Much like the resistivity, the thermopower or Seebeck coefficient is an intrinsic property of a material and it is related to its electronic structure. However, unlike the sample's resistance, it is known that the Seebeck coefficent is a geometry independant thermodynamic property. The thermopower of the device is given by the ratio of the sample's voltage to the temperature gradient:

$$\alpha_{SP} = \frac{\Delta V}{\Delta T} = \frac{(V_H - V_L)}{(T_H - T_L)} \tag{2.8}$$

where $\alpha_{SP} = \alpha_P - \alpha_S$ is the measured value of the thermopower. Here α_P represents the probe's contribution and α_S (or the sample Seebeck coefficient S) the sample's contribution. The probe's contribution must be known and subtracted. Often, this lead contribution is significantly low as compared with the sample's contribution, allowing us to use a differential method of measurement. Eventually, the lead contribution can be neglected [98].

Reference [99] predicts that the sample's thermopower ($\alpha_S = \alpha_P - \alpha_{SP}$) will typically be opposite in sign from the measured thermopower, because the probe's contribution is often small compared to the sample's thermopower. For optimal accuracy, extra care should be taken in determining the temperatures as closely as possible from the voltage probes. There are essentially two ways to detect thermal anchoring problems in the setup, which unfortunately is one of the

common causes of inacurracy. An important time lag in change of temperatures between the sample voltage and thermocouple voltage suggests unwanted thermal inertia, which is a symptom of improper thermal anchoring. Additionally, a large difference in thermopower when measuring it at atmospheric pressure and under vacuum also indicates a poor thermal anchoring.

There is are number of methods for measuring the thermopower, which can be classified primarily into two groups; AC and DC measurements. DC measurements are direct current measurements. They are usually fairly simple to operate. Nonetheless, they need a relatively long waiting time for the temperatures to stabilize across the sample. This makes the measurement tedious in case one desires to collect the thermopower values for a large spectrum of temperatures. AC measurements involve alternate current setups. This method allows faster results and offers greater accuracy, especially for ranges when S varies drastically as a function of temperature. AC techniques require special care and complex setups. For this reason, the AC measurement technique will not be discussed further as emphasising on DC methods seems more pertinent.

The simplest of DC methods involves heating one side of the sample to a fixed temperature. It creates a natural temperature gradient within the sample. This gradient is then measured using thermocouples. An alternative technique consists in establishing a small fixed gradient of temperature ($\Delta T/T$ = a few percent) and varying T slowly. For each value of T, the thermopower is calculated using the relationship $\alpha_{SP} = \frac{\Delta V}{\Delta T}$.

Since the latter method adds in complexity due to the controlled and precise application of not one but two heat sources, our focus will remain on the former, namely the method in which a natural gradient is created in the device because of a single heat source.

The object of this study is to explore the Seebeck coefficient of Ge NWs embedded in an oxide matrix. The way it is done in practice is equivalent to exploring the effect of Ge nanowires on the Seebeck coeffient of a thin-film oxide.

To eliminate the detrimental impact of undesirable effects, such as poor thermal anchoring or Seebeck effect in the probes, it is best to use a comparative method. Instead of performing, on a single sample, direct absolute measurements that would include undesired data, comparative methods use two samples, a control sample, and the sample of interest. Usually, the sample of interest differs in composition or properties. It is always the effect of this sample difference that is meant to be measured. Applied to our case, one sample consists of embedded nanowires, and it is the sample of interest. A sample with same oxide thickness and composition, but without the nanowires, will serve as the control sample. As a consequence, the difference in Seebeck coefficient between the control sample (without NWs) and that with NWs represents the Seebeck coefficient of NWs.

2.7.1 Integrated Heater Technique

Measuring directly the Seebeck coefficient perpendicular to thin film devices is particularly difficult because it is difficult to establish a temperature gradient accross the film while simultaneously measuring localized temperature and voltage change [100]. Accurate local temperature measurements can be achieved by integrating, on top of the NW matrix, a thin-film metal wire that serves both as a thermometer and a heater [98] [100]. We use a simplifying hypothesis which is to neglect all thermal resistances between the device and the measurement tools such as thermocouples and voltage probes. The method proceeds in two steps.

Step 1 – Determine $\mathbf{R_{th}}$(Device)

Initially, a known heat load[3]($Q = R(T) \times I^2$) is applied on top of the wafer through the integrated heater. The same heater also serves as a thermometer where T_h, the temperature at the top of the device, is obtained by measuring $R(T)$ in the heating electrical circuit. It is assumed that the heater was pre-

[3]where $R(T)$ is the electrical resistance of the heater at temperature T

viously characterized, meaning that the correspondance between its resistance $R(T)$ and the local temperature T is known. Measuring the bottom temperature of the sample (T_s) yields the value of the temperature gradient across the whole device $\Delta_T(Device) = T_h - T_s$. This can be done with a simple external thermocouple. It is important at this stage to emphasize that $\Delta_T(Device)$ is different from $\Delta_T(Film)$, which is the temperature gradient across the sole thin film. The latter would be expressed as $\Delta_T(Film) = T_h - T_{s'}$, where $T_{s'}$ is the temperature at the interface between the Si sample and the heat sink of the device. Simplified models show indeed that $T_{s'}$ differs from the sink's temperature T_s [98]. Then, the thermal resistance of the whole device $R_{th}(Device)$ is obtained by simple calculus: $R_{th}(Device) = \frac{\Delta_T}{Q}$. This step would usually be performed once. For later calculation purposes one must know the thermal resistance of the sample itself.

Step 2 – Measure Intermediate Values

- Measure ΔV
- Measure T_h and T_s
- Calculate $T_{s'} = T_s + \frac{R_{th}(Si)}{R_{th}(Si)+R_{th}(Film)} \times \Delta T$,
  where $R_{th}(Si)$, is the substrate's thermal resistance. It can be found in the literature to be 157.0 K/W [98] but might depend on sample properties such as carrier concentration and crystalline orientation.
  Also, in practice, we use $R_{th}(Device)$ instead of $R_{th}(Si) + R_{th}(Film)$.

Step 3 – Extract S_{Film}

S_{Si} is the substrate's Seebeck coefficient. It found either in the literature [101] [102] [103] or in the Si wafer datasheets.

Having all the above values, the following equation must be solved to extract S_{Film} [98]:

$$\Delta V = S_{Si} \times (T_{s'} - Ts) + S_{Film} \times (T_h - T_{s'}) \tag{2.9}$$

On the possibility to extract thermal conductivity

While exploring this method, it was observed that this generic method proposed by Zhang *et al.* [100] can be extended in order to extract, with no extra procedure, the value of the perpendicular thermal conductivity. Indeed, in the thermal model proposed by Zhang *et al.*:

$$R_{th}(Device) - R_{th}(Si) = R_{th}(Film) \tag{2.10}$$

The perpendicular thermal conductivity of the thin film can in fact be calculated using the following popular thermal equation:

$$k(Film) = \frac{1}{R_{th}(Film)} \times \frac{d}{A} \tag{2.11}$$

where d is the thin film thickness and A is the surface area of the thin film.

2.7.2 Simultaneous Resistivity and Seebeck Coefficient Measurements

Equation (2.7) was expressed in a way to extract the resistive part of voltage induced by opposite DC currents across the device. Analogously, one can extract the value of the Seebeck coefficient of the device:

$$V_{TE} = \alpha\Delta T = \frac{[V_{IR}(I^+) + \alpha\Delta T] + [V_{IR}(I^-) + \alpha\Delta T]}{2} \tag{2.12}$$

In other words, it is possible within two consecutive voltage measurements, where two opposite DC current sweeps are passed through the sample, to extract the resistivity and the Seebeck voltage of the whole device. It must be emphasize that this technique yields the Seebeck coefficient of the whole device and not that of the sample alone nor the thin film alone. This being said, in order to retrieve the film's or sample Seebeck voltage, a comparative method using two devices can be used as described in Section 2.7.

3. Experimental Details

3.1 Intended Device Structure

The schematic structure of the intended devices is shown in Figure 3.1.

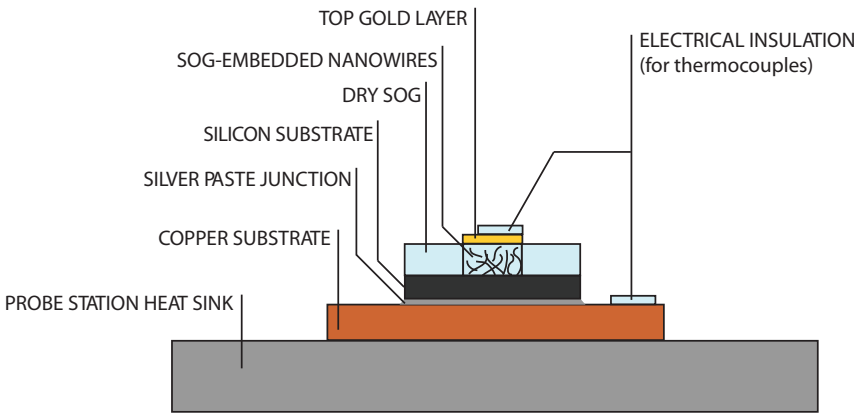

Figure 3.1: Schematic cross-section of the intended device

The intended device is composed of a substrate of copper, acting as a heat sink. Copper is indeed a very good thermal and electrical conductor. On top of it, the silicon sample is permanently mounted using silver paste due to its good electrical conductivity as well as good thermal conductivity. Near the silicon substrate, a thin pad of spin-on-glass (SOG) is placed to provide electrical (but not thermal) insulation. This SOG pad is later used for thermocouple-based

temperature measurements described in Chapter 5.

The copper heat sink used in the device has a square shape (about 25 mm $\times$ 25 mm) and a thickness of 2 mm.

3.2 Sample Preparation

The samples selected for the following study have the following properties:

- Material: Silicon
- Doping type: Boron (B) – p-type
- Resistivity: [0.85-1.15] Ω.cm
- Crystallographic orientation: <111>
- Brand: Walker
- Sample size: 1cm $\times$ 1cm
- Wafer thickness: 275 μm
- Wafer diameter: 2 inches

The silicon substrates systematically undergo two ultrasonic bathes, 15 minutes in acetone. This is followed by a nitrogen blow-dry. The sample is then sonicated for 15 minutes in isopropyl alcohol (IPA) before undergoing another blow-dry. This process is instrumental in clearing most sources of contamination.

The silicon substrates are then dipped into a solution called amino-propyl trimethoxysilane (APTS), that helps the subsequent gold (Au) colloid deposition process. APTS is a patented solution that was developed to provide a monolayer interface allowing Au nanocolloids to chemically bond stably onto the silicon sample's intrinsic oxide layer. A 0.05% - diluted APTS solution is used to soak the samples for 10 minutes, before drying the sample using nitrogen.

The next step consists in depositing gold colloidal onto the sample. To achieve different densities, one can vary the dipping time into the solution. The highest densities are obtained by leaving a drop of gold colloidal to dry onto the sample. In our case, a dipping time one of one to two hours of is sufficient to obtain a satisfactory density of gold dots.

After dipping in gold colloid, the sample is blown-dried and kept in a clean dry box until use for growth. The available sizes of Au colloids were 20 nm and 50 nm.

3.3 Device Fabrication

3.3.1 Nanowire Integration

The SOG used is HONEYWELL ACCUGLASS 211. It must be noted that its expiry date was January 7, 2006 which corresponds to a use 3 years after expiry date. The product however still presented all desirable properties that can be expected from such a material.

The typical recipe set for applying the SOG with the spinner was 500 rpm, reached in 1 second, half the desired final speed, reached in one second, the the final speed reached in one second, and maintained for the desired duration. To stop the spinner, it is set to decelerate totally (0 rpm) in 2 seconds. The spinner used in this study is the SPINCOATER Model P6700.

Since the length of the NWs resulting from vapour transport growth is of the order of tens of microns, it would be naive to expect the SOG to fill it in at the bottom of the NWs without affecting the shape of the wires. In practice, Ge NWs seem to be an extremely flexible structure. Different micrographs in Chapter 4 show indeed the spaghetti-like behaviour of NWs in a liquid environment. After spinning, the NWs are flattened down and embedded in a thin SOG layer.

With high densities of NWs, SOG in pure form did not fill the bottom part of the NWs, instead it left an empty layer of air above the sample that contributed

to a highly cracked surface after baking. Different dilution ratios were experimented so as to vary the SOG viscosity and thus filling ability. With a dilution of 50% into IPA, the surface after spinning was inhomogeneous regardless of the spinning speed. The problem was overcome by using a dilution ratio of 75%, meaning 3 parts of SOG for one part of IPA. A comprehensive presentation of the integration of NWs can be found in Chapter 4.

3.4 Nanowire Growth Furnace

The process used for Ge NW growth is chemical vapour deposition (CVD) by vapour transport. The growth mechanism that is intended is vapour-liquid-solid (VLS).

The furnace model that was used is the Lindberg/Blue STF55346C. It is composed of three independant heating sections as shown in Figure 3.2.

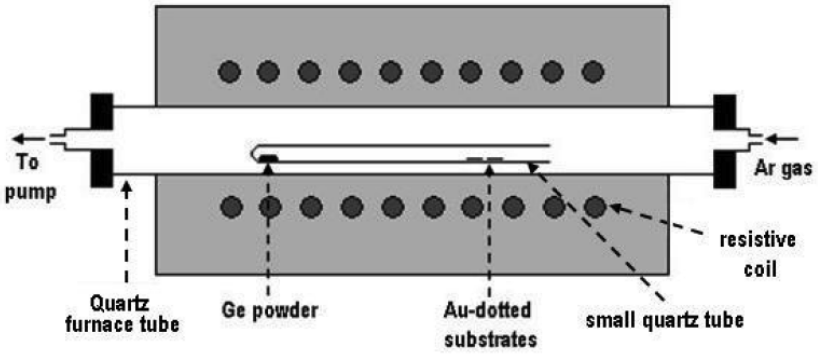

Figure 3.2: Schematic cross-section of the growth furnace

A ceramic boat is filled with a small amount of Ge nanopowder (half a small plastic coffee spoon, about 300 mg). The boat is then inserted to the farthest inside a quartz test tube while the sample is placed a few centimeters away from the opening of the test tube.

The precise location of the boat, also called crucible, and of the sample, are meant to match the position of the respective centers of the heating zones.

The quartz test tube is then placed inside the ceramic furnace tube. The ceramic tube is then sealed and pumped down to 2.66 mbar. A controlled flow of

Argon gas is then used at rates between 100 sccm and 300 sccm.

Various markers were used to ensure the consistent positioning of the crucible and sample in the quartz test tube, and also of the quartz test tube in the furnace tube.

When the desired pressure and gas flow are reached, the heating process starts. The typical ranges of temperatures that were used are from 810 to 950°C in the heating zone containing the boat, 630 to 775°C in the center heating zone, and 450 to 600°C for the heating zone containing the sample. Temperature differences of above 200°C between two consecutive zones are not advisable as the quartz test tube cannot withstand such large gradients.

The establishment of the growth set of temperatures takes from 40 minutes to one hour when temperature ramps up from room temperature (25 °C). The time for which the desired temparatures are reached and kept stable depends on the desired length of nanowires. As for the cooling process, the furnace is usually set aside to cool down in air for one hour, although in practice it takes longer to reach an acceptable temperature that makes it possible to unseal the furnace tube.

Ideally at the beginning of the cooling stage, the ceramic heat insulators at both ends of the furnace tube are removed for quicker cooling. When the maximum temperature inside the furnace goes below 200°C, a pressure slightly above atmospheric pressure is established in the furnace tube by simple argon filling. Then, the tube can be opened, but it was not systematically opened immediately after argon filling.

3.5 Scanning Electron Microscope

The scanning electron miscroscope (SEM) used is the Philips XL30. It is systematically used between key steps of the fabrication process to examine the sample so as to ensure its control over the experimental conditions. The SEM was typically used after the deposition of gold preceding a growth, after growth, and

after curing the SOG. A charging phenomenon was observed under the SEM while visualizing the sample after SOG deposition. This is due to the dielectric nature of SOG. The only possible way that the SEM may affect the sample is by unintentional carbon contamination. Basically, in the SEM chamber there are traces of residual gases, e.g. hydrocarbon. The energy from the electron beam could cause the carbon from these gases to be deposited onto the sample. Nothing in the whole present study suggested such contamination.

Typical acceleration voltages that were used range between 10 and 30 kV and the sample was placed at a distance of 20 to 30 mm away from the final lens. Angles of inclination ranged from 0 (perpendicular to sample) to 85 degrees (near to visualizing cross-section).

3.6 Heating Station, Probe Station and Parameter Analyzer

The probe station that was used is a typical black chamber equipped mainly with a heating stage connected to an external heater, and with adjustable probe tips connected to an external parameter analyzer. Other accessories include an optical microscope for the correct positioning of the probes onto the sample, a light source with adjustable power, and an adjustable gas flow system that blows argon around the sample to avoid condensation in the sample area.

The model of the heater is the Temptronic ThermoChuck TP03000A. It can be operated at temperatures between -65°C and +200°C. The temperatures used in this study are between -40°C and +150°C. This non-exhaustive range was chosen due to particularly long delays in establishing extreme temperatures, particularly the cold ones.

The temperature establishment within the samples was yet another time consuming process. It takes typically 15 to 25 minutes to obtain stable sample temperatures, besides the 5 to 10 minutes required to change temperatures. It is best

to begin with the lowest temperature, and increase temperature until reaching the maximum desired temperature for the sample of interest. Another approach could consist of establishing a given temperature, and use it for all the samples before changing temperatures. This approach was excluded for the experimental conditions as a given sample would change at each temperature. Mounting and unmounting the probe tips would indeed induce a different electrical contact at each temperature, for each sample.

The parameter analyzer that was used is the model HP 4155B. It is composed of several Source/Measurement Units (SMUs). From the point of view of the parameter analyzer, the probe tip connected to an SMU can serve as a source, or as a source and a measurement unit. The SMU can be used as a voltage or a current source. The analyzer allows several modes of operation, mainly the sampling mode and the sweep mode.

In the sampling mode, the source value is constant and other SMU values are recorded versus time at the desired frequency.

In the sweeping mode, the source value can be swept, meaning incrementally increased or decreased at a chosen frequency, and other SMU values are recorded at each step of the sweep.

In our particular case, in order to apply the alternate DC current method described in section 2.7.2 on page 44, there is no need for the sweeping mode. The SMU was used as a current source and a voltage probe. Alternatively, the current source value (5 μA), was set to the negative value, according to the Seebeck coefficient measurement technique mentioned earlier. This value was chosen for a device area of about 1cm^2, in order to avoid breaking down the oxide layer. For an oxide film a few microns thick, current densities below 10 μA / cm^2 are considered relatively safe.

A manipulator probe in the probe station, connected to an SMU, was used to probe the gold contact area on top of the sample. The circuit was closed by connecting the stage chuck to the parameter analyzer and setting to ground.

When the parameter analyzer is used as a current source, no current can be established in a closed loop, hence the technical impossibility for this current measurement to assess the electrical noise voltage, also called the baseline noise. Measuring this baseline noise consists in operating a given measurement circuit under the voltage-sweep mode to measure the noise voltage. It is important in any measurement to be able to assess the background noise impact.

3.7 Temperature Measurement

The temperature measurements were performed using independent temperature measurement devices. Two identical FLUKE multimeters combined each to two identical k-type FLUKE thermocouple modules (model 80TK) were used.

The thermocouples were meant to measure a temperature difference as precisely as possible. Therefore, one thermocouple was adjusted on the other. In practice, at each temperature, the two thermocouples were placed at the exact same location on the copper base. In such conditions, the temperature is expected to be the same. Tough, when the displayed temperatures differed, the bias of a given thermometer with respect to the other one was stored, and used to compensate its values. Thus, although it is not an absolute temperature calibration, this relative compensation is sufficient when the aim is simply to collect a temperature difference. The compensations for one thermocouple with respect to the reference thermocouple were of +0.4K at -40°C and -0.4K at +40°C.

3.8 Transmission Electronic Microscope

The transmission electronic microscope (TEM) is used to confirm that the nanowires obtained are single-crystal Ge nanowires.

The silicon sample was immersed in 50 microliters of ethanol and sonicated in a ultrasonic bath for 5 minutes. Afterwards, the ethanol solution containing nanowires was transfered onto a TEM grid using a micro-pipette.

Figure 3.3 shows a typical image of one such single-crystalline nanowire. The nanoparticles at the tip of the wires generally appear dark and have high contrast compared with the nanowire. A high-resolution TEM image (Figure 3.4) shows the atomic lattice.

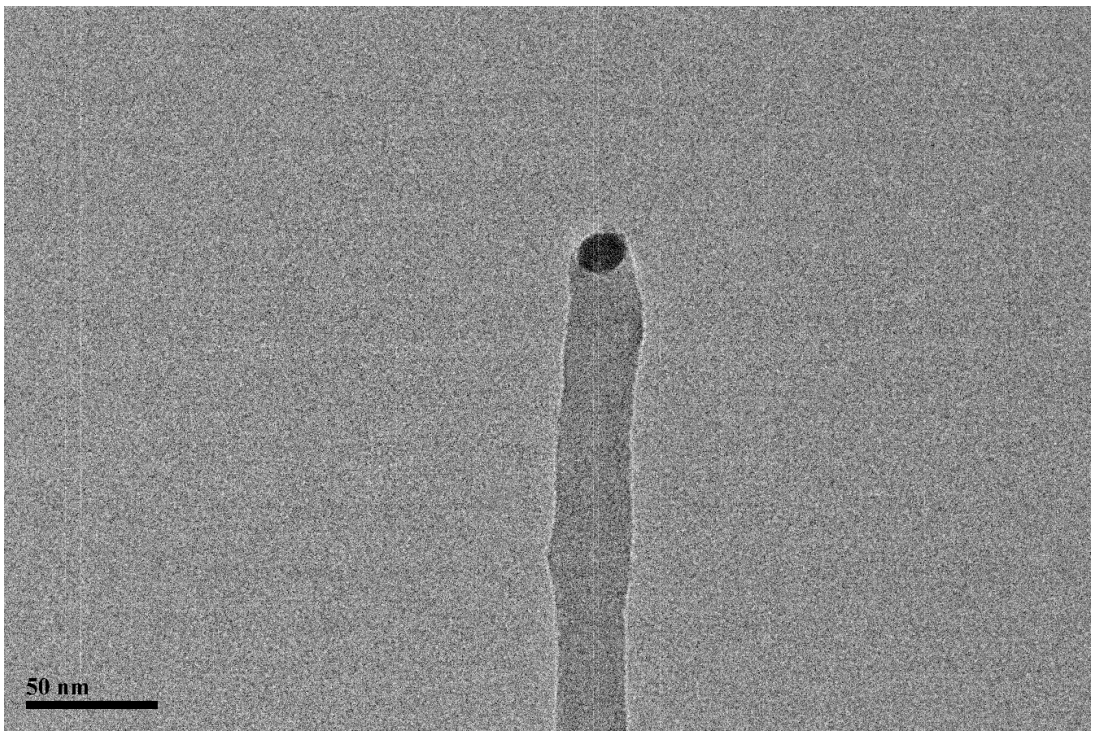

Figure 3.3: A typical TEM image of germanium nanowire with diameter of about 35 nm. The scale bar corresponds to 50 nm. Top inset shows an Au/Ge alloy cluster at the tip of a wire.

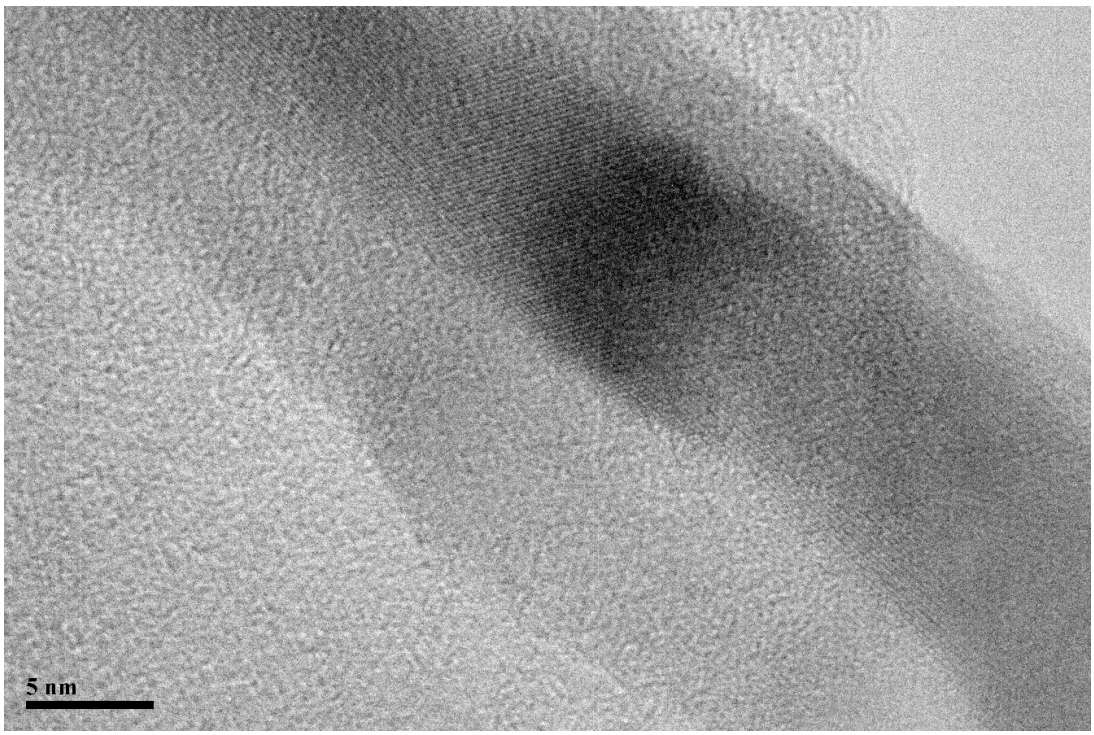

Figure 3.4: A high-resolution TEM image on a 15-nm Ge nanowire. The scale bar corresponds to 5 nm.

4. Growth and Fabrication of Germanium Nanowires

4.1 Introduction

Initially, the focus was to perform the Ge NW growth onto stainless steel (SS) substrates.

SS is meant to provide a heat sink and a rigid mechanical support. Ideally the heat sink material should have a high thermal conductivity so that the overall thermal conductance of the structure is dominated by that of the Ge NW layer. SS has a reasonably high thermal conductivity, which is close to that of silicon. Unlike silicon, SS is stronger and not as brittle. Although SS does not have as high a thermal conductivity as some metals like copper, it does not oxidize as easily as copper. This is important so that the interface formed when integrating the Ge NW layer onto the substrate will not present a poor thermal conductance, so as to dominate that of the overall structure, and mask out the effect of the GE NW layer.

The use of SS as a substrate for monocrystalline semiconductor growth is little documented. Successful results, involving mainly the fabrication of lithium batteries, were published [104] [105] and served as a base for start. Critical diffi-

culties were encountered in the experiments using SS substrates, leading attention to focus on a more practical alternative.

Various highly doped silicon substrates were used and led to successful growth of Ge NW with interesting properties in terms of density and diameter.

However, yet new difficulties arose in the process of integration for the Ge NWs into a spin-on-glass (SOG) matrix. This lead to a series of trial and error experiments, by experimenting with factors such as the dimensions of the Ge NWs, the viscosity of the SOG solution, or the spinner settings.

When successful integration was obtained, the devices were further processed in order to create electrodes and prepare them for thermoelectric characterization.

4.2 Results

4.2.1 Ge nanowire growth on stainless steel substrates

Stainless steel in bulk form, unless polished, presents a particularly rough surface, as compared with the more standard semiconductor substrates. A first investigation consisted in testing gold colloidal adhesion on a rough-surface metal like SS. Figure 4.1 shows an SEM view of the surface of a typical unpolished SS sample. A closer view, in Figure 4.2 shows a typical micrograph of the adhesion of gold colloid on the surface of SS unpolished samples. The colloids are present on the sample, which proves the ability of adhesion of Au colloids on SS. Besides, they do not specifically accumulate inside the surface defects. This suggests a colloid spacial distribution comparable to that of polished semiconductor substrates. It is indeed important that the colloids do not merge together so that growth can occur.

Two different sizes of gold colloids s (20 nm and 50 nm diameter) were applied on SS substrates to determine the most suitable size given the growth temperature set (920°C at the source, 530°C on the samples, for 60 minutes, with

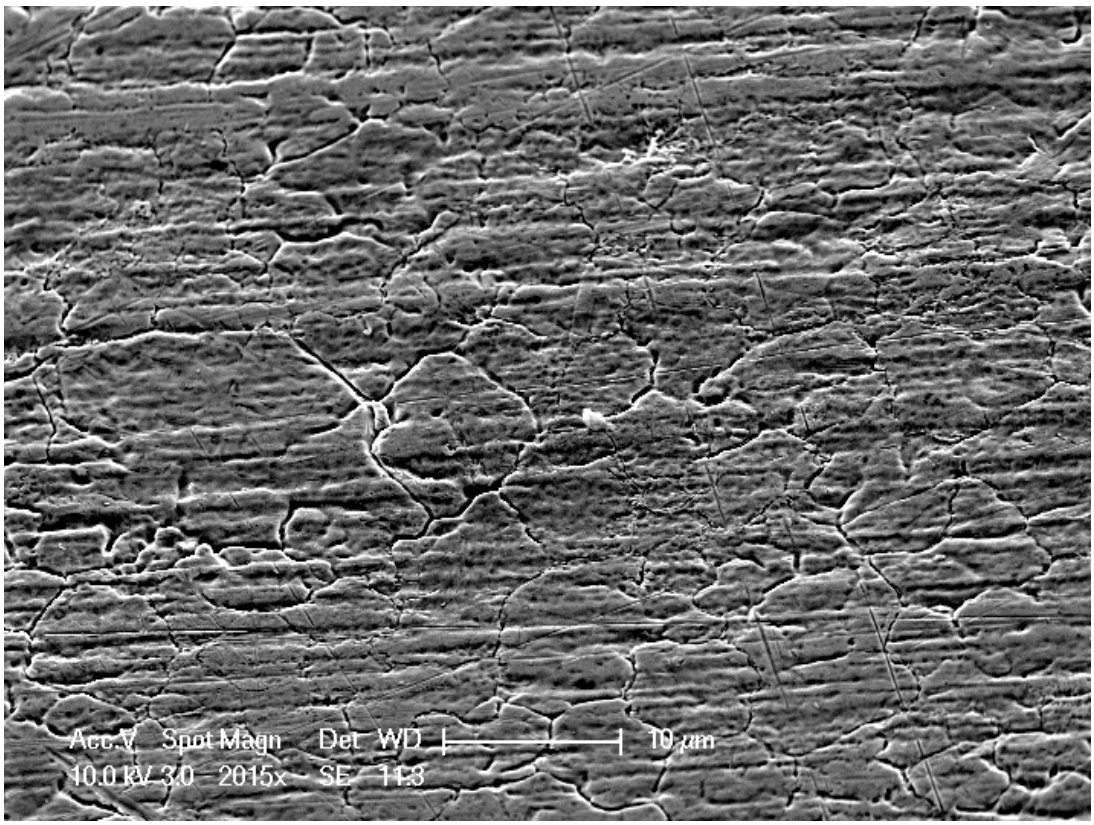

Figure 4.1: SEM view of the surface of a typical unpolished SS sample

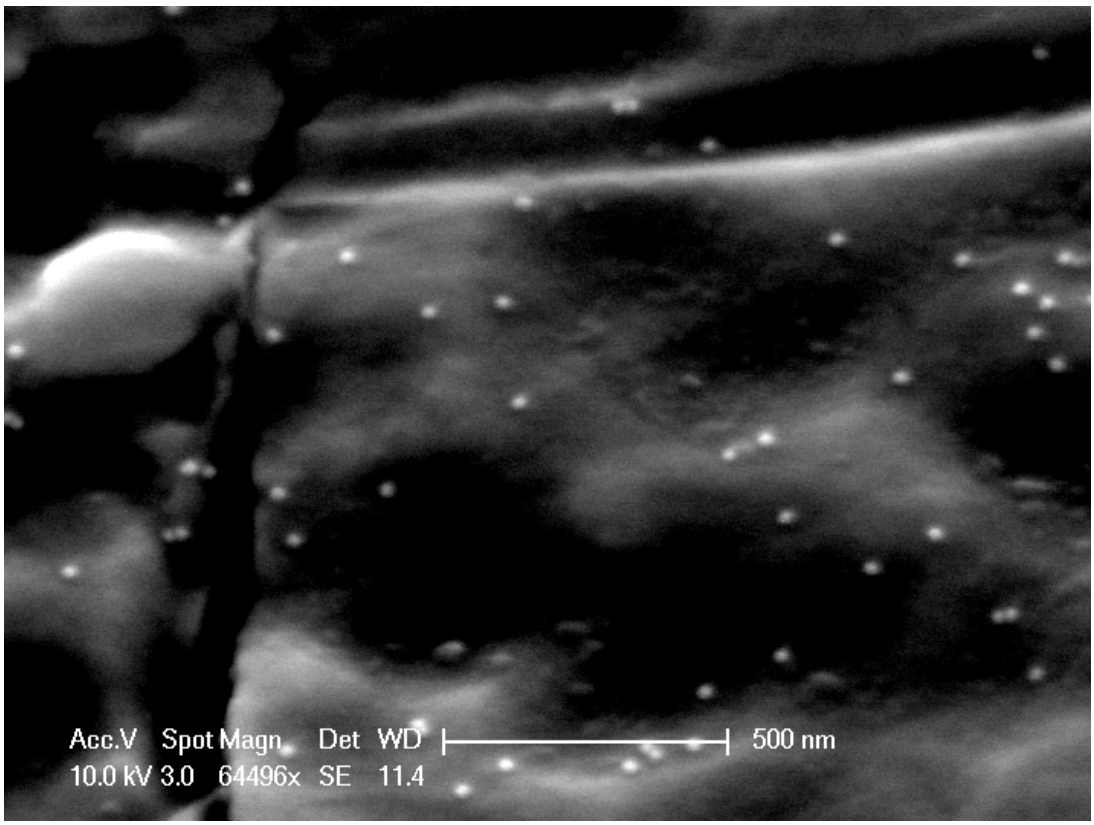

Figure 4.2: SEM view showing gold colloids adhesion on the surface of a typical unpolished SS sample

an argon flow of 150 sccm and a partial pressure of 2.66 mbar). Although relatively better densities were observed with 20 nm diameter gold colloids, the Ge NW growth remains poor whether 20 or 50 nm diameter gold colloid is used. The SEM micrographs in Figures 4.3 and 4.4 show that although gold colloids are fairly uniform prior to growth, they tend to form clusters at higher temperatures. This clustering may result from the movement of melted gold colloids down to the fissures and other interstices between bumps. This phenomenon of clustering is widely known to prevent normal Ge NWs growth since the seeds become very large.

The diameters of the NWs were also explored and revealed fairly large nanowires. Figure 4.5 shows the typical diameter of a Ge NW grown with 20 nm diameter gold colloids; it shows a diameter close to 100 nm. Figure 4.6 shows the typical diameter of a Ge NW grown with 50 nm diameter gold colloids. The diameter is larger and ranges above 150 nm. The large diameters with respect to the size found in a reference study [105] of Ge NW growth on polished SS, which revealed values of 50-100 nm for comparable sizes of gold colloid. The larger diameters support the hypothesis that clustering occurs. Besides preventing growth, even the smaller clusters affect the nanowires that grow successfully by providing them with an excessively large diameter which may be detrimental to good TE performance.

Despite many adjustments of density and growth conditions, rough bulk unpolished SS offers poor perspectives in terms of density of the Ge NWs. For this reason, it was decided to explore more conventional substrates, such as silicon.

4.2.2 Ge nanowire growth on doped silicon substrates

Conditions of successful growth

The first attempt of growing Ge NWs on silicon samples was successful density-wise. Like it was done with SS substrates, two different diameter gold colloids were experimented, 20 nm and 50 nm. Figures 4.7 and 4.8 show respectively

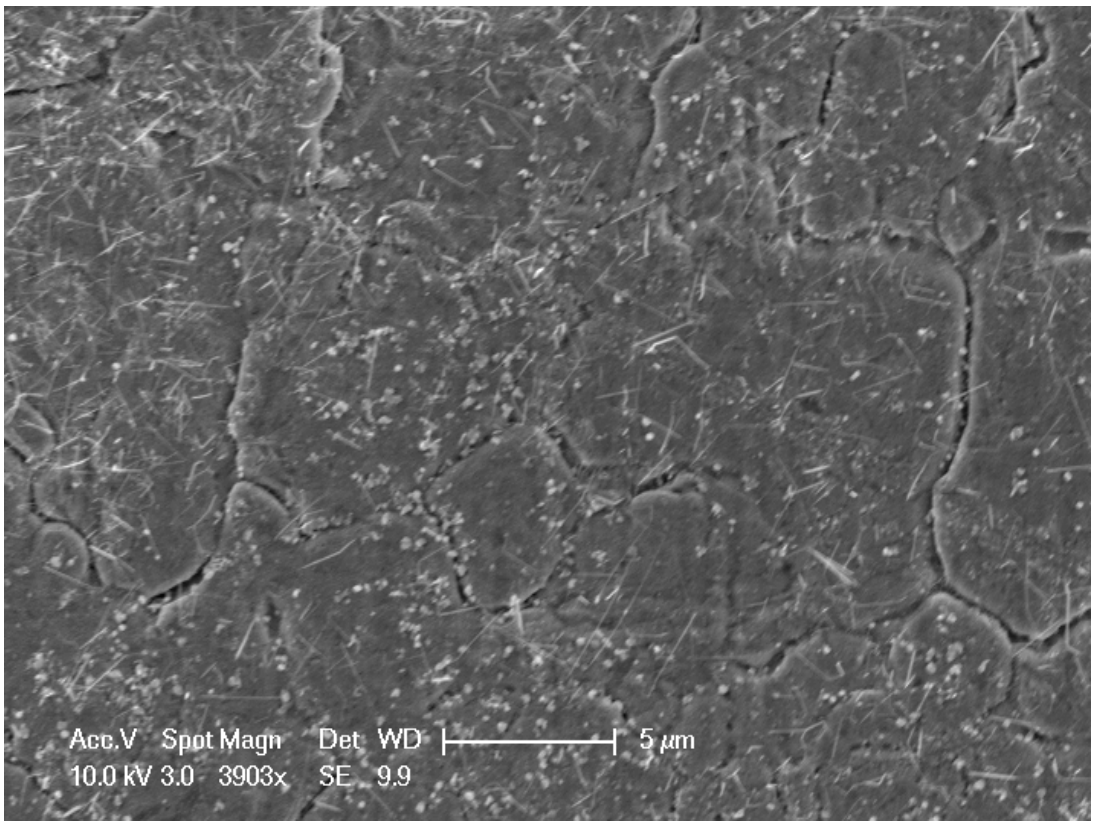

Figure 4.3: SEM view of typical growth results of Ge NWs (white elongated structures) on SS using 20 nm diameter gold colloid

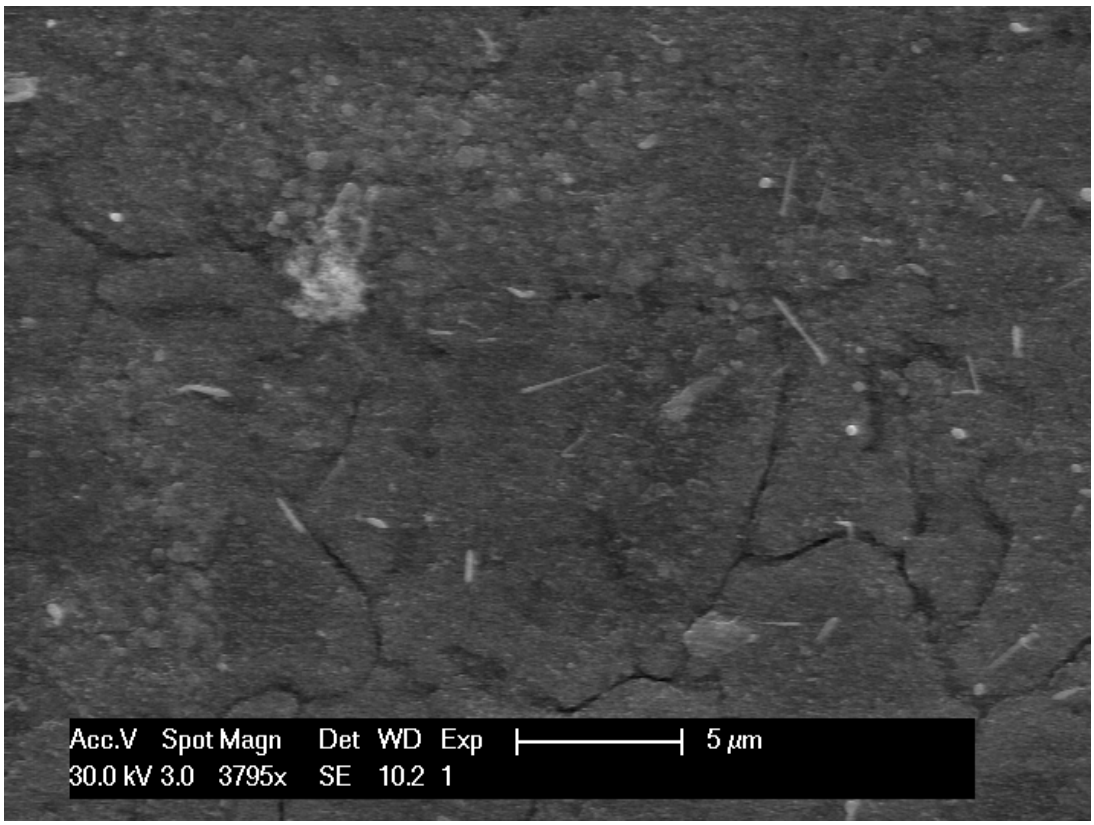

Figure 4.4: SEM view of typical growth results of Ge NWs (white elongated structures) on SS using 50 nm diameter gold colloid

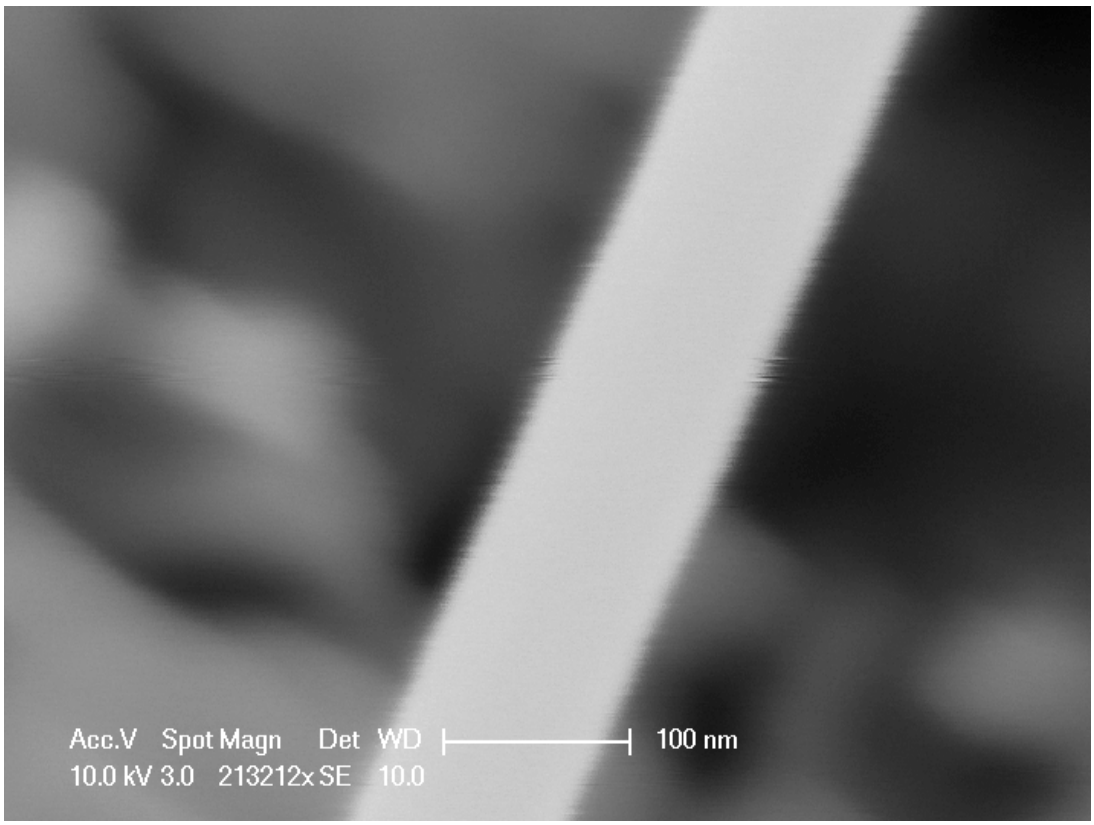

Figure 4.5: Magnified SEM view of the typical diameter of Ge NW grown an SS substrate with 20-nm gold colloid

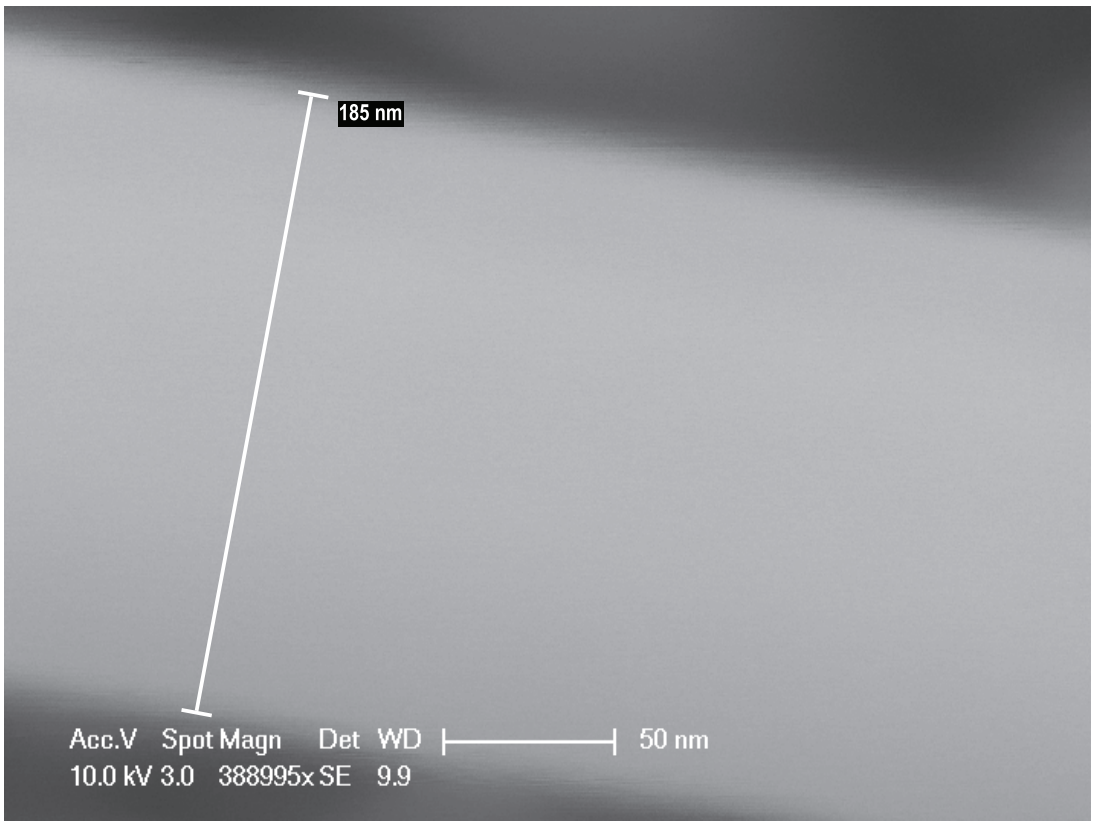

Figure 4.6: Magnified SEM view of the typical diameter of Ge NW grown on an SS substrate with 50-nm gold colloid

the results of each size. NWs grown using 20 nm diameter gold colloids are more uniform than those grown using 50 nm diameter gold colloids. This is due to a phenomenon called tapering, caused by radial growth, and causing the wires to be conic instead of cylindrical. In other words, for the specific set of experimental conditions that were used, 20 nm was the most suitable gold colloid size. The experimental conditions were as follows: source (zone 1 of the furnace) was at 920°C, samples (zone 3) at 530°C, intermediary zone (zone 2) was at 720°C, the heating stages (heating, maintaining, cooling) lasted respectively 60 minutes, 40 minutes, and 60 minutes. A constant flow of Ar at 150 sccm was used in the furnace tube throughout the whole process. The density of the gold colloid was normal, as it was left on the sample for about 2 hours before being blown-dried. These conditions may be referred to further on as the basic growth conditions.

Particular cases

Interestingly, extremely high densities of gold colloids, created an unexpected result that might be interesting for TE applications. Indeed, when the colloids were applied onto the samples until fully dry, the same basic conditions lead to very different forms of nanowires. Figures 4.9 and 4.10 show cubic nanostructures that are along the nanowires. As mentioned in the literature review, because these objects are defects along the nanowires, they may contribute to the TE effect by creating obstacles to the linear transport of phonons. The process of how these cubic nanostructures are formed along the Ge NWs is not fully understood presently. It remains of interest to compare the thermoelectric properties of these wires with cubic nanostructures with the thermoelectric properties of more standard Ge NWs.

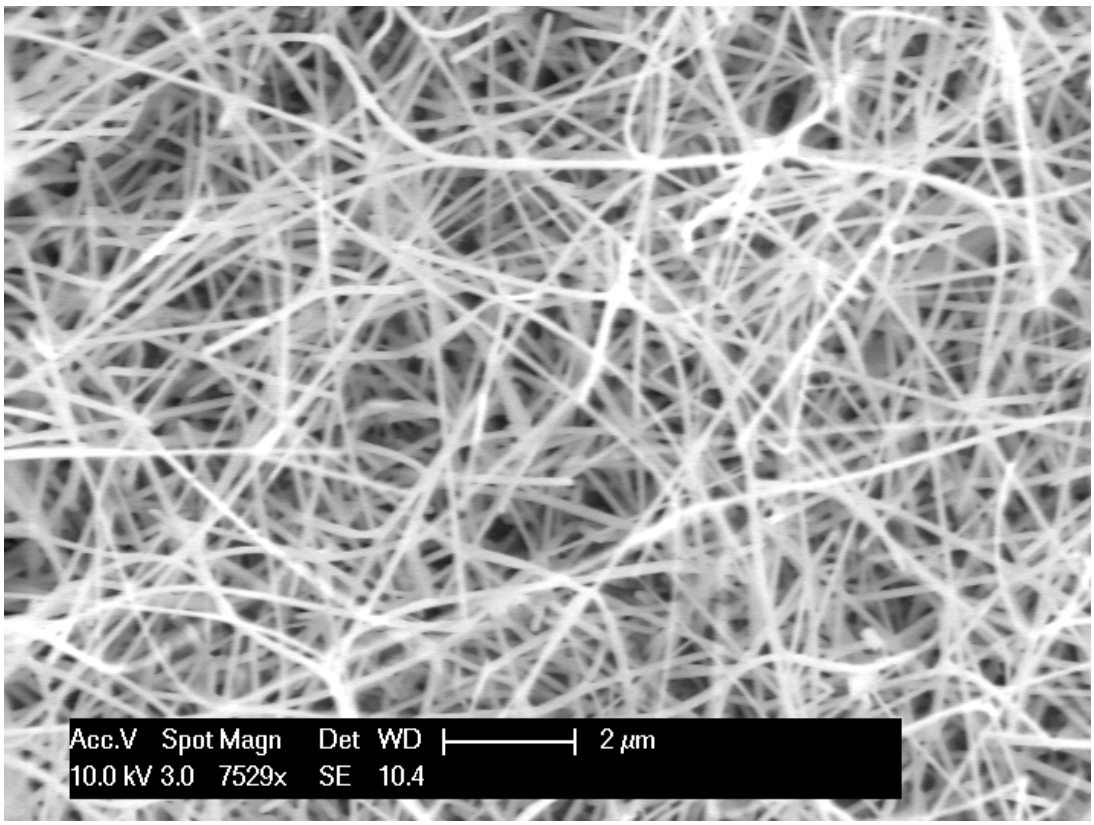

Figure 4.7: Typical SEM view of Ge NWs grown on an Si substrate with 20-nm gold colloid

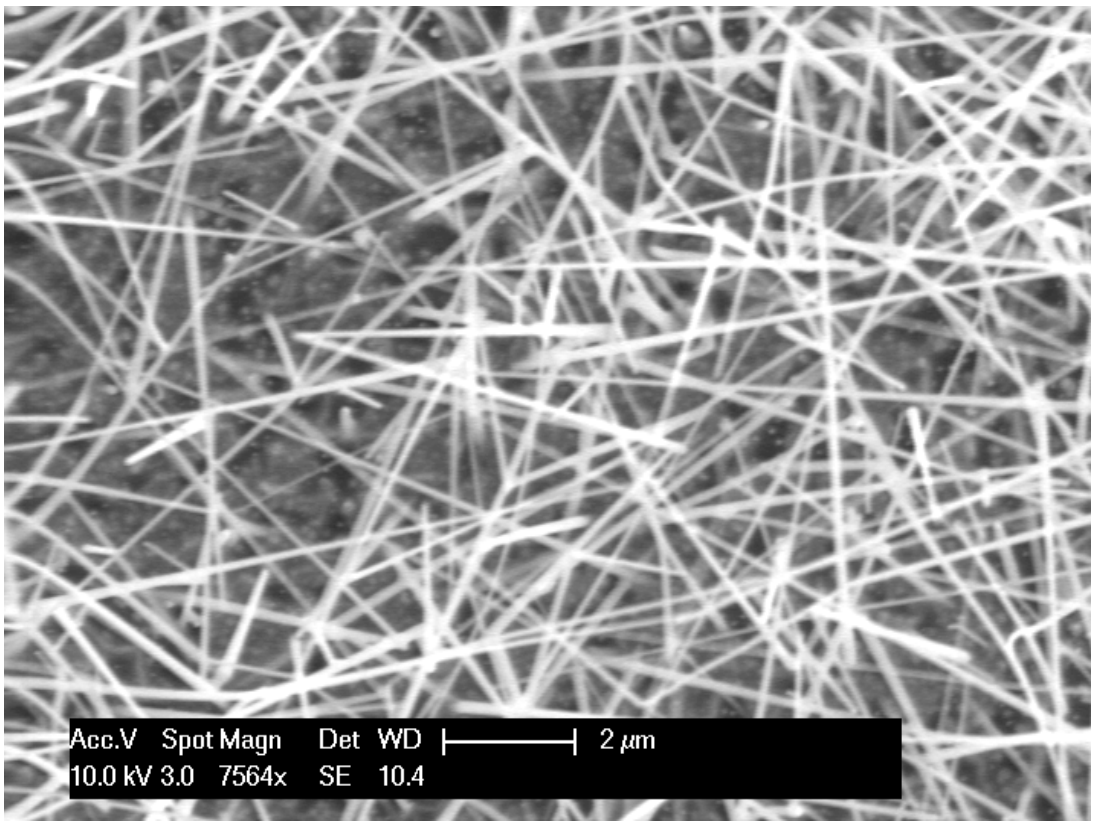

Figure 4.8: Typical SEM view of Ge NWs grown on Si substrate with 50-nm gold colloid

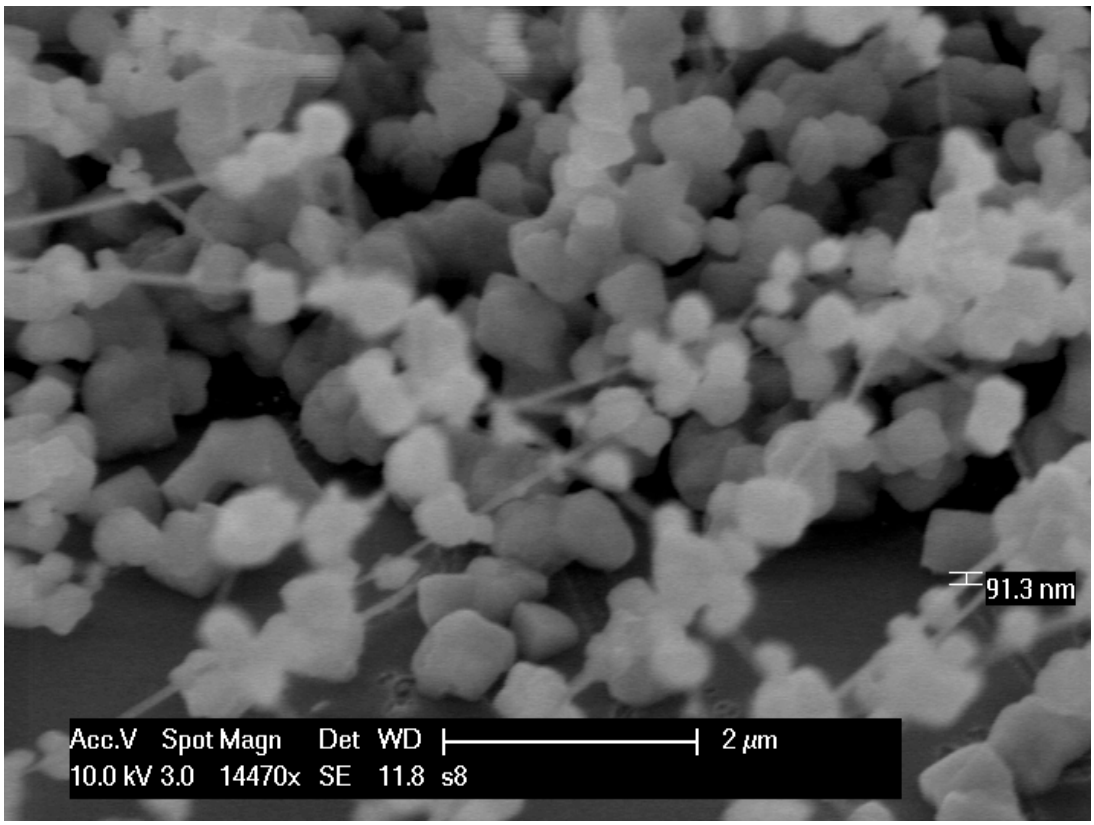

Figure 4.9: SEM top view of cubic forms along Ge NWs at extremely high gold colloid densities

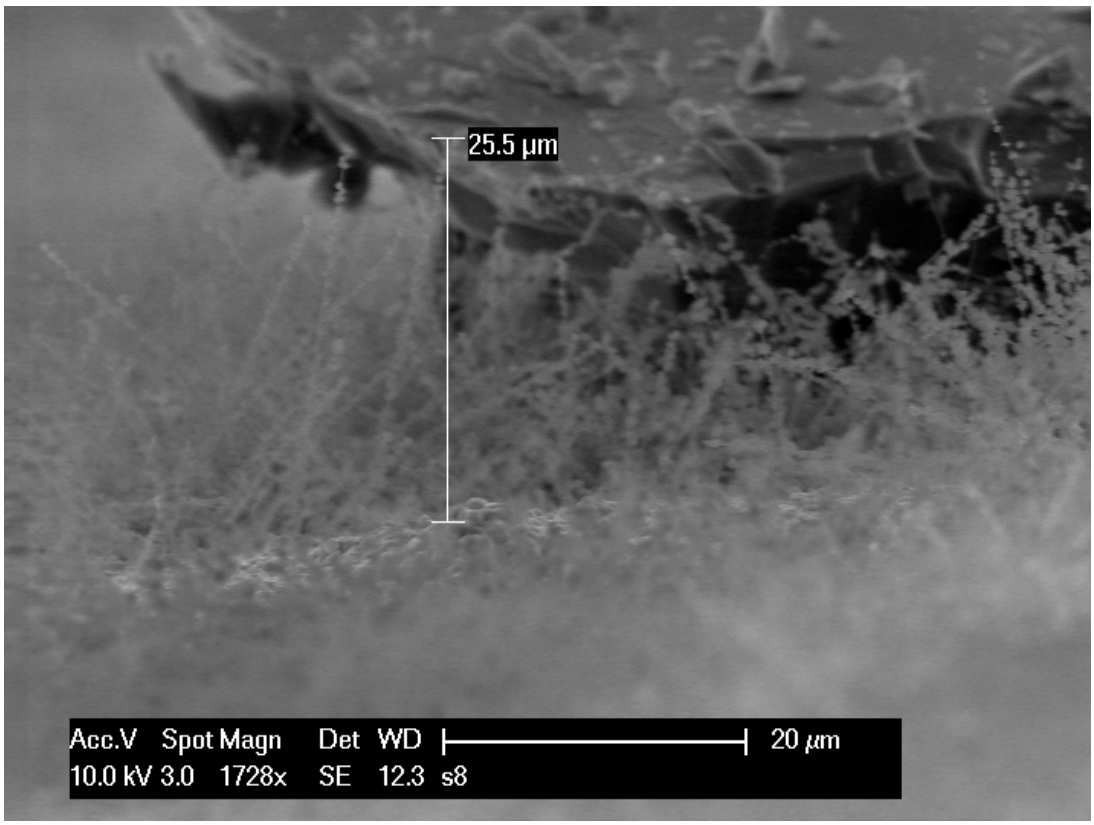

Figure 4.10: SEM side view of cubic forms along Ge NWs at extremely high gold colloid densities

4.2.3 Device Integration

The step of device integration consists of embedding the previously grown NWs into an oxide. In the present work, it was chosen to do so with spin-on-glass (SOG), a mix of silicon polymers and solvents, that polymerizes to become solid when being baked.

Embedding issues

From the first attempts to embed the NWs, emerged a serious problem to tackle. A typical sample using the basic growth conditions was taken (see Figure 4.11). SOG, spinned at about 2000 RPM onto the silicon substrate with Ge NWs, and then baked, resulted in important surface cracks, as shown in Figure 4.12. Figure 4.13 offers an even closer view. The latter is instrumental in explaining the problem and thus leading to a solution. It can be seen that the SOG does not penetrate down to the bottom of the NWs, at the interface with the silicon substrate. Most of the SOG is therefore attached to the NWs but barely to the silicon substrate. It therefore dries and hardens itself, probably breaking some NWs in the process. Possible solutions to this issue may involve making the SOG fluid less viscous so that better filling can take place. Besides, tests of SOG deposition were performed on samples without Ge NWs, and pure SOG resulted in a thin layer with good uniformity and no cracks (see Figure 4.14). So the cracks are not exclusively due to the viscous nature of the SOG but also to the presence of NWs. Hence, another path to solve the cracks problem, consists in easing access of the SOG to the silicon substrate, primarily by reducing the length of the Ge NWs.

4.2.4 Towards integrable TE-relevant Ge NWs

A series of incremental changes in the growth process has permitted to grow short nanowires (1 to 2 microns) , with smaller diameters (about 30 nm). This

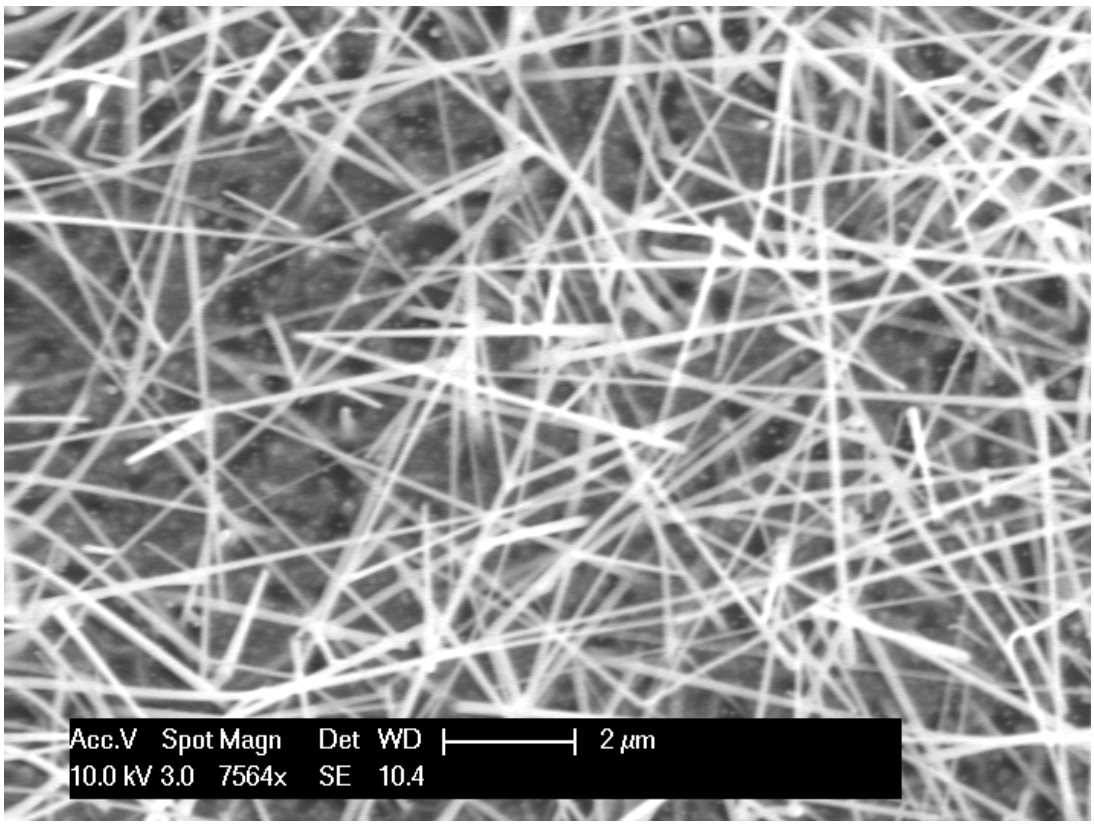

Figure 4.11: SEM view of a standard sample with Ge NWs, prior to SOG application

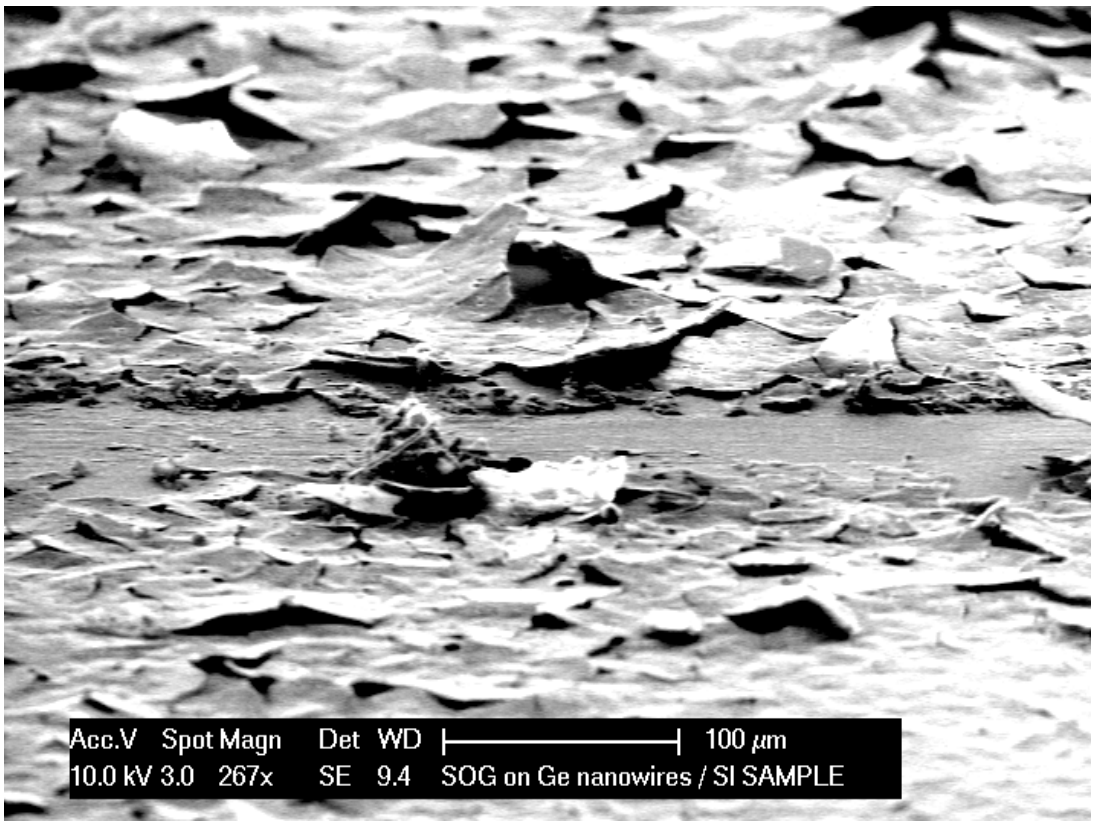

Figure 4.12: Large SEM view of the surface of a sample with Ge NWs, after SOG application and bake

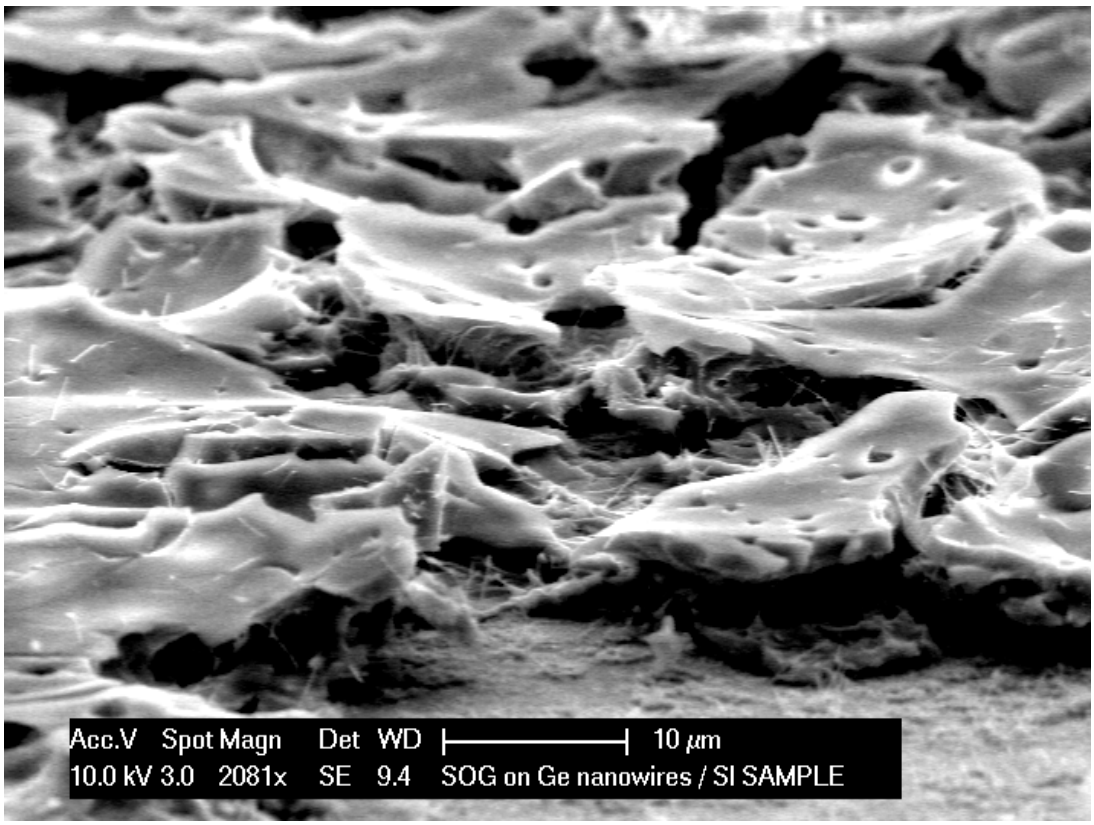

Figure 4.13: Closer SEM view of the surface of a sample with Ge NWs, after SOG application and bake

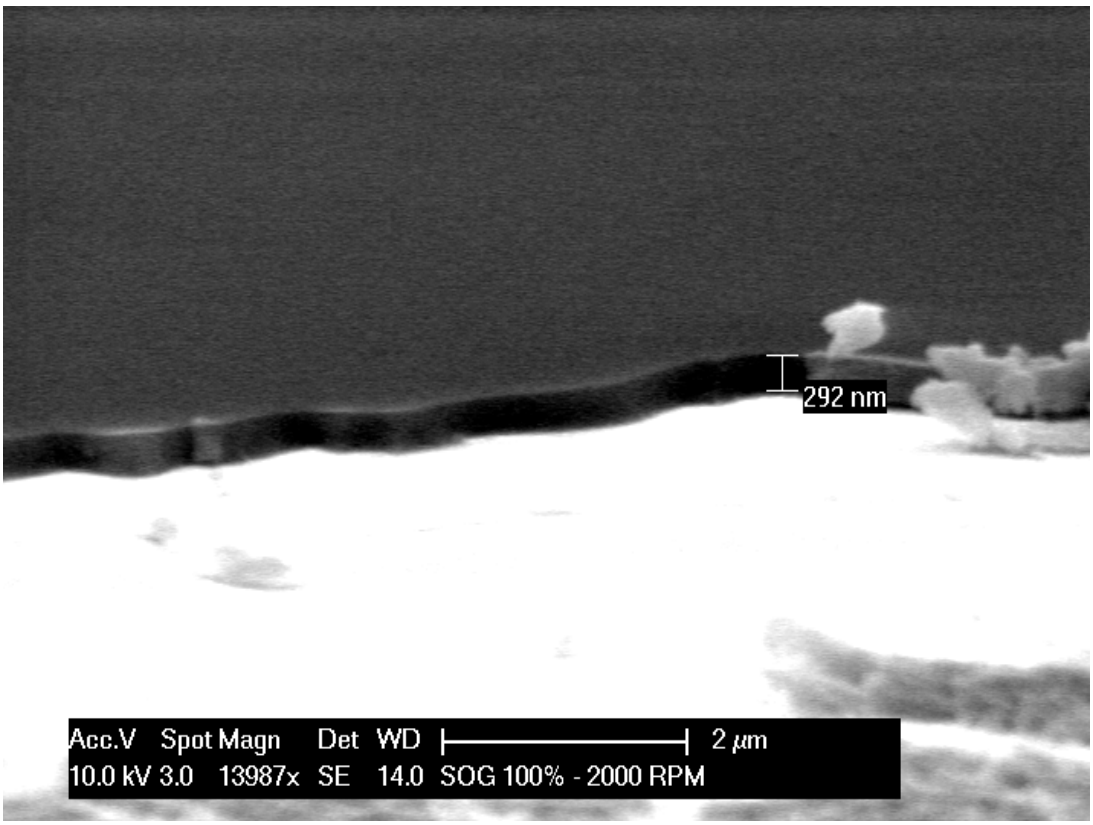

Figure 4.14: SEM view of the surface of a sample without Ge NWs, after SOG application and bake

made integration into SOG possible, without cracks or major surface defects.

A first approach in making the NWs shorter consisted in reducing the growth duration, mainly the constant-temperature regime after the temperature ramp up, as it seemed to be when most of the growth occurred. Using the former basic growth conditions yielded NWs which are a few tens of microns long, with the constant-temperature regime lasting 40 minutes. It was therefore expected that a change of constant-temperature regime duration from 40 minutes to 8 minutes would shorten the NWs from a few tens of microns (10-40 microns) to less than 10 microns. The result however did not support this expectation, exhibiting yet relatively long wires (15-35 microns) as can be seen in Figure 4.15.

Knowing that growth length is directly impacted by growth duration, the only reason why the wires were not significantly shorter than usual can only reside in an error of hypothesis. In fact, the hypothesis that most of the growth occurs essentially during the constant-temperature regime was likely to be false. Although germanium's melting point is 938.3°C, germanium evaporation may start to occur at lower temperatures. This means growth may begin while the furnace temperature is progressively increasing and still continues at the initial period of the cooling stage. If this was the case, the growth duration with the basic growth condition would not be 40 minutes but say 82 minutes. As a consequence, the change that was made (reducing the "growth" duration) did not transform 40 minutes but 80 minutes of growth, into not 8 but $8 + 42 = 50$ minutes of growth. The ratio of time reduction would be a lot smaller than expected, and would result in little change in the wire length.

To verify this new hypothesis, one may lower the growth temperature. This way, the overall evaporation duration is shortened. Figure 4.16 on page 77 reminds the structure of the conventional growth furnace by showing a schematic cross-section diagram.

The new experiment was performed with identical duration as previously (60 min., 8 min., 60 min.) but the set of temperatures was changed from (**920**,

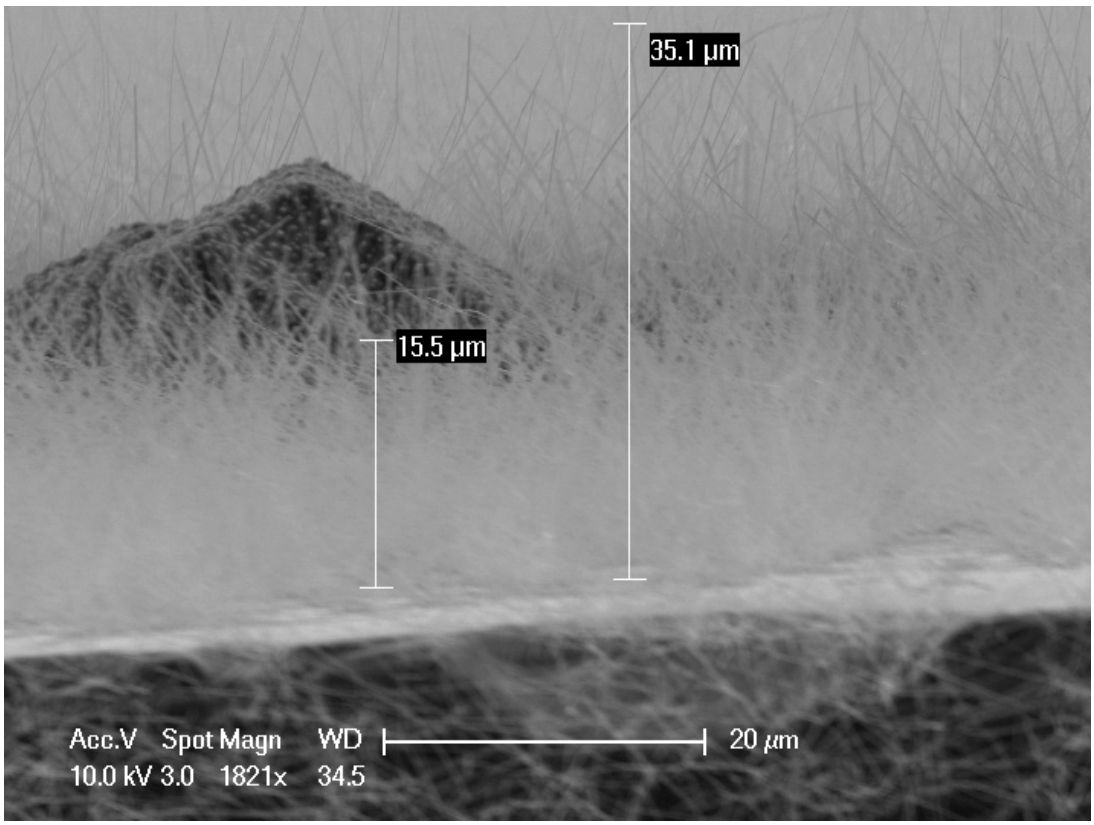

Figure 4.15: Cross-section of NW sample following reduction of growth duration

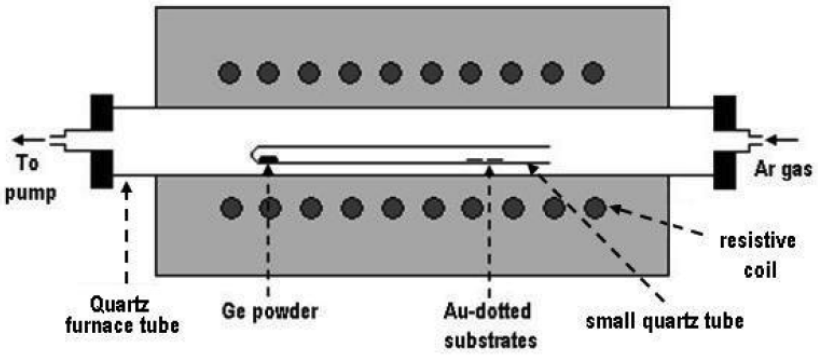

Figure 4.16: Schematic cross-section of the growth furnace

720, 530) to (**810**°C , 650°C , 530°C). The average NW length was significantly reduced from 15-35 microns to 5-13 microns (see Figure 4.17). It must be noted that not only the evaporation time is shorter, but lower temperatures induce lower liberation of Ge vapour, hence a lower growth rate.

In order to ensure short NWs as far as possible, another path to length reduction was considered. In previous experiments, the argon flow was permanent. Besides being an inert gas used for low pressure control in vacuum systems, argon in our case may also promote growth. In fact, the flow of argon takes place in the opposite direction to that of the quartz test tube. In other words, the argon counters the Ge vapour flow and may prevent it from escaping from the test tube. This means that the argon flow may increase the probability that a Ge vapour particle will deposit on a gold colloid instead of escaping from the test tube. To enhance this effect, the pressure setting was also changed. The manometer valve was fully open to let the pressure go as low as possible while the temperatures were increasing. Once the constant-temperature regime began, argon was then let in at a pressure of 2.66 mbar and flow rate of 150 sccm. It was pumped later when cooling began. This was to prevent growth from occurring outside the constant-temperature stage. Finally, the heating and cooling durations were changed, from 60 minutes to 30 minutes. The result was repeatable and presented in Figure 4.18. The figure shows that combining the reduction of source temperature, growth duration, and argon flow, reduces significantly the length of Ge NWs. Because several parameters were applied concurrently, the

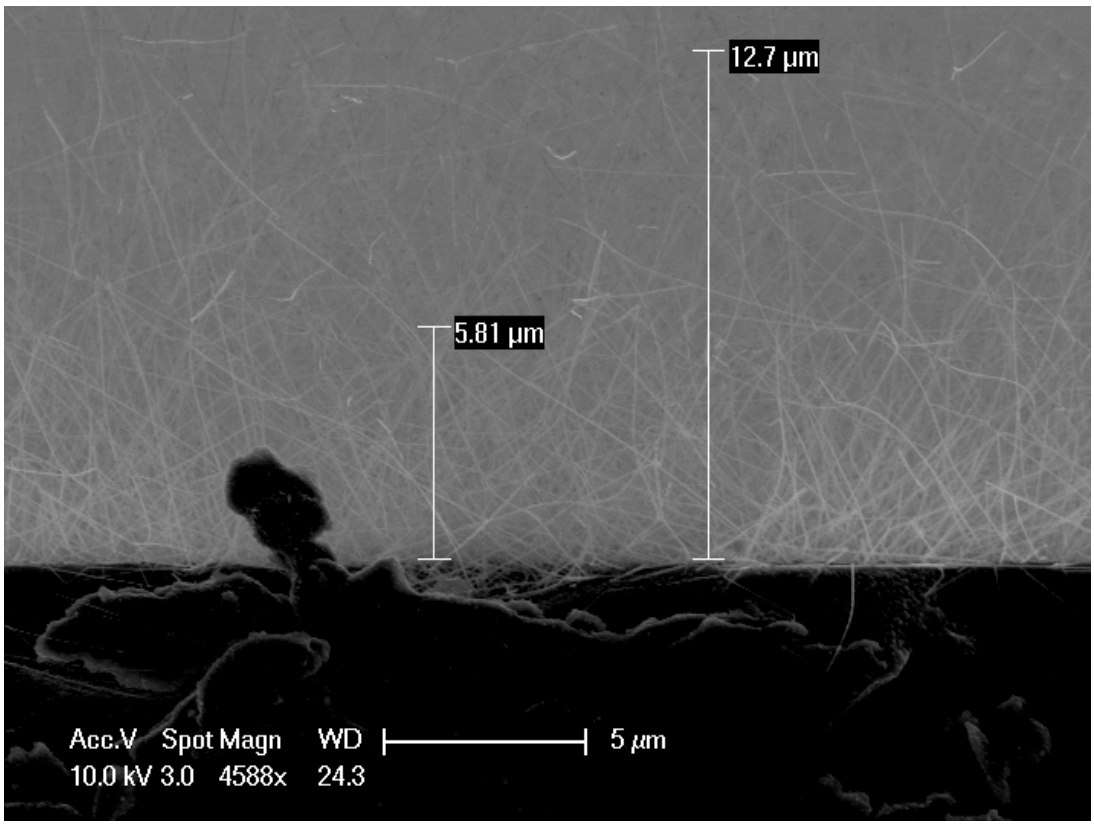

Figure 4.17: Cross-section of NW sample following reduction of growth duration and source temperature

contribution of each remained at this stage unclear. However, wires of only a few microns long were obtained with this process.

To assess the effect of argon flow, further experiments were carried out, and led to the conclusion that the above explanation on the effect of argon may not be entirely correct. As presented in Figure 4.19, a repeatable process grew NWs of the similar short length with a **permanent** argon flow at 150 sccm. The recipe used a temperature setting of (810°C , 630°C , 450°C) and the following heating stages (25 min., 30 min., 25 min.).

4.3 Final SOG integration results

Combining the use of short nanowires obtained with the processes above-described, and a 50% dilution of the SOG fluid, resulted in a major increase in the usability of the device. Figure 4.20 shows the surface of the device after SOG application and cure. There are no visible cracks, but irregularities can be observed. Figures 4.21 and 4.22 show closer views of the top surface of the devices. It is possible to see some NWs embedded into the SOG, but it is not necessary that all NWs should be visible since many may be flat against the substrate or simply below a thicker amount of SOG. These figures also show the thickness differences within the sample. These are normal and inherent to the spinning of SOG on a NW surface and can be suppressed using chemical-mechanical polishing (CMP)[94]. The laboratory did not have such equipment. It was therefore decided to complete the integration of these devices despite their thickness irregularities and to proceed further with the Seebeck coefficient measurements.

4.4 Summary

Although SS is a potential substrate for Ge NW growth for TE applications, growth of Ge NWs on this unconventional substrate did not yield uniformly and sufficiently dense NWs. Though the NW growth may have been more straight-

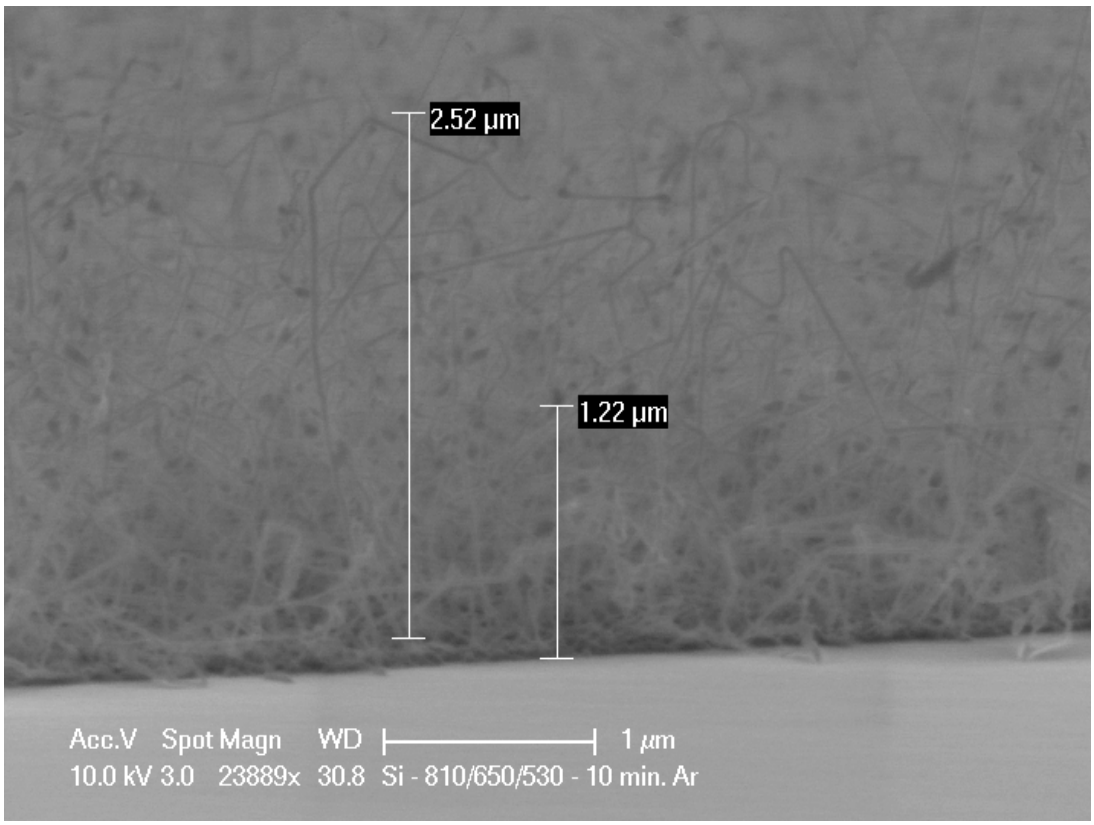

Figure 4.18: Cross-section of NW sample following reduction of source temperature, growth duration and argon flow

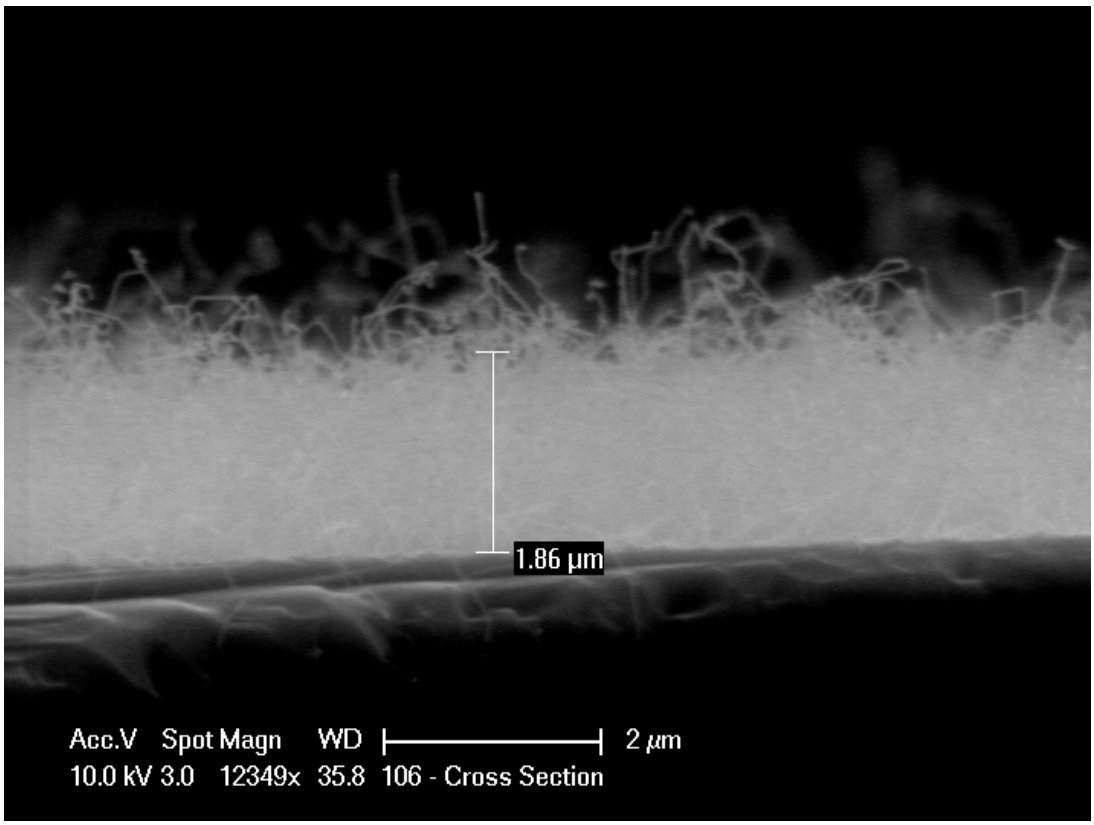

Figure 4.19: Cross-section of NW sample following reduction of source temperature, sample temperature, with permanent argon flow

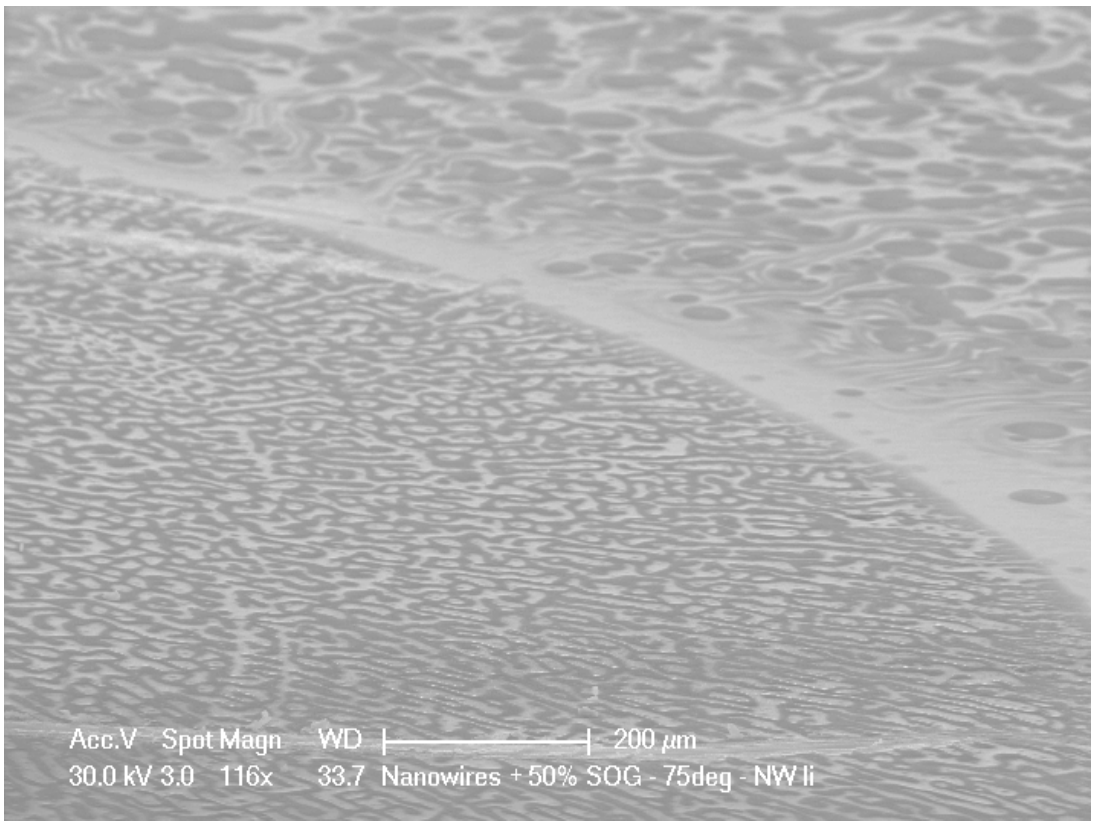

Figure 4.20: Integration of short nanowires using 50% diluted SOG

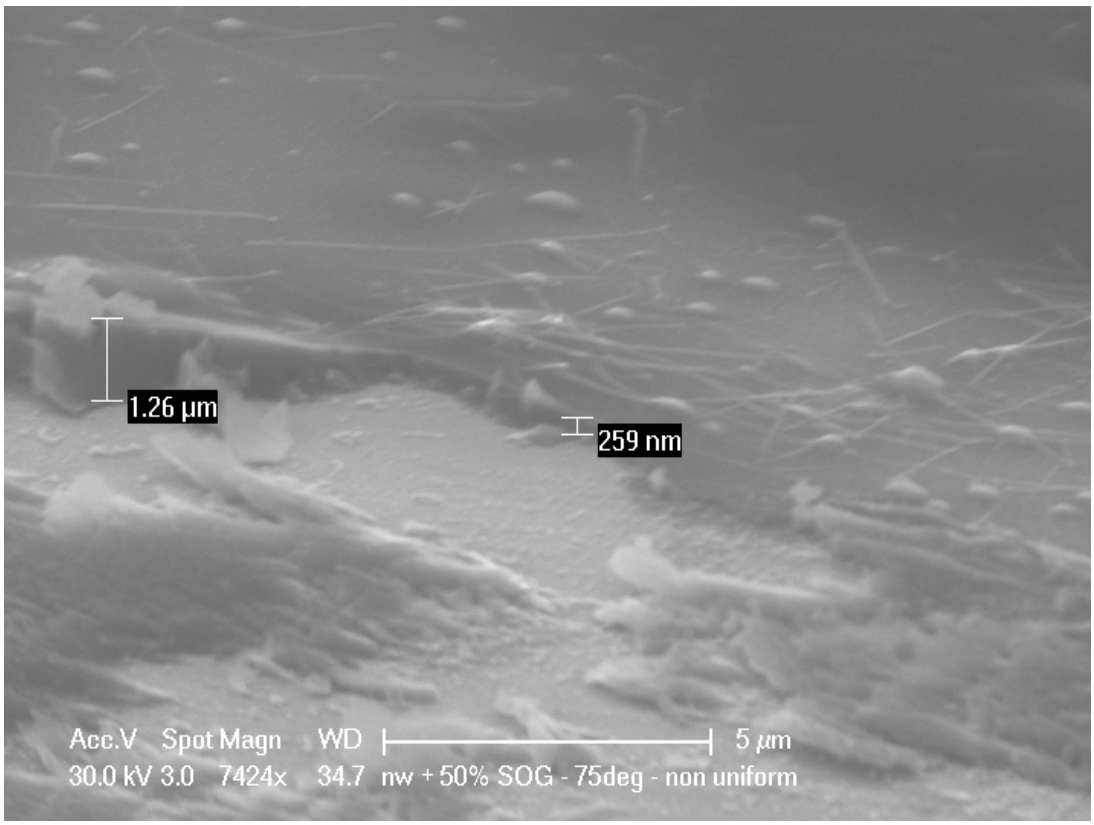

Figure 4.21: Embedded NWs and thickness variations

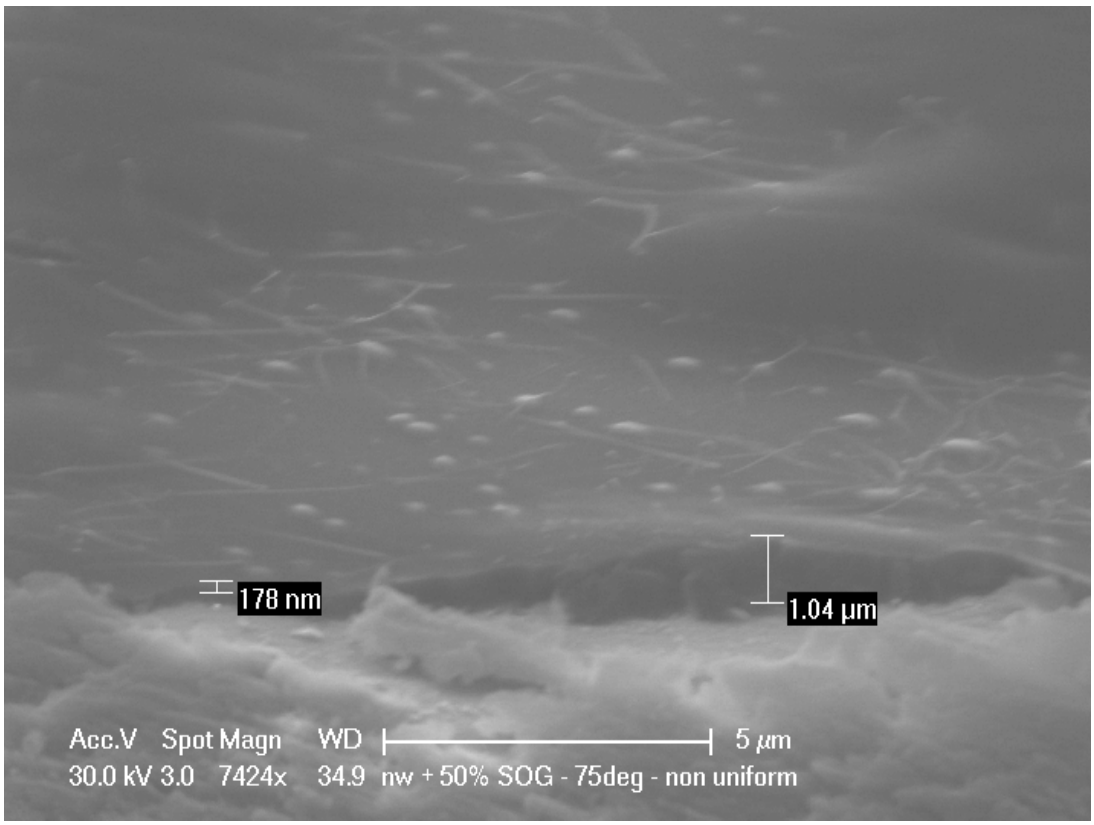

Figure 4.22: Embedded NWs and thickness variations (different view of the same sample)

forward on silicon substrates, long nanowires were not desirable as they prevent SOG from filling the interstices down to the substrate surface. Accordingly with the literature review, it was possible to shorten the Ge NWs from tens of microns to a few microns by reducing essentially the growth temperature (source and eventually sample) and the growth duration.

5. Measurement of Seebeck Coefficient

5.1 Introduction

The experimental setup for the measurement of the Seebeck coefficient is presented in sections 3.6 on page 50 and in section 3.7 on page 52. The following explains the process of data retrieval and analysis.

Three devices were used, 2 devices with Ge nanowires, and a control device without nanowires. Schematic cross-sections of the devices in question can be found in Figure 3.1 on page 45. In the following, these devices are denoted as DEV1, DEV2 and Control device.

Two measurement temperatures were used, -40°C and +40°C. These are arbitrary, nothing in the Seebeck measurement method obliges to take opposites values nor positive and negative values.

For each device and at each temperature, a constant current was applied for 2.5 seconds for the positive half-cycle. The current polarity was reversed for another 2.5 seconds for the negative half-cycle, according to the method described in Sections 2.7 and 2.6. For each half-cycle, 125 voltage data points were measured, along with the temperature across the device, through two thermocouples linked each to a multimeter for display. The temperature values could not

be recorded in real time and were thus read and noted manually during the voltage measurement. The values are then stored in a CSV file onto a floppy-disk.

The above-described process is performed overall for 6 times: The first time a positive current is applied. The second time, a negative current is applied, thus forming a cycle. Two more of these cycles terminate this series of 6 half-cycles. It must be noted that the 6 half-cycles were measured individually. The time delay between two consecutive half-cycles is 10 to 15 seconds. For obvious display reasons, these waiting times will not be represented on the plots, but it may be important to remain aware of this point.

The files were all imported and compiled into a matrix. The values of the temperatures were updated to account for the temperature differences that were noticed during the calibration of the thermocouples.

A script was written to calculate the statistics on the Seebeck coefficient and the resistance of the devices.

Firstly, for each half-cycle, the average voltage value is calculated. This is primarily because the calculation method requires only one value of voltage for each half-cycle. Since the voltage values fluctuate, the mean was taken for calculation. This value was called V_{mean}.

Secondly, for each half-cycle, based on the top and bottom temperatures, the temperature difference across the device is calculated. This value was called ΔT for each half-cycle.

Thirdly, for each half-cycle, the resistance value is calculated. Based on equation 2.7 on page 39, the resistance is calculated according to:

$$R = \frac{[V_{mean}(I^+) - V_{mean}(I^+)]}{2 * I} \tag{5.1}$$

where I is the magnitude of the current bias for each half cycle.

Note that this calculation does not require the knowledge of the temperature difference.

Fourthly, the Seebeck cofficient is calculated. Like the resistance calculation,

this calculation requires the voltage values of a full cycle. However, it also required the temperature difference **over the full cycle**. Because these values can differ within a cycle, they are first averaged to allow for a single value, as needed in the following equation:

$$\alpha = -\frac{[V_{mean}(I^+) + V_{mean}(I^+)]}{2 * \Delta T} \tag{5.2}$$

Note also that all temperatures differences and potential differences (Seebeck voltages) are obtained by subtracting the bottom values to the top values. For instance, $\Delta T = T_{top} - T_{bottom}$, the same applies to voltages.

5.1.1 Proposing an alternative method

Flowing a current through a thermoelectric device results in the establishment of a voltage of resistive and thermoelectric origin. Extracting these values allows one to calculate the resistance of the devices, and the Seebeck coefficient, which are two major factors in the assessment for the thermoelectric performance of a device. In order to do so, the method used in this work required opposite polarities but identical magnitudes of current. In the mathematical sense however, these two unknown variables, resistive voltage and thermoelectric voltage, do not require that the currents are necessarily opposites. Indeed, the use of a similar equation with different values is sufficient to reveal the two unknowns as the number of equations equates the number of unknowns. Another equation can be obtained with simply a different current value.

Based on this observation, sweeping a current was considered and tested on Device 1. By sweeping a current, the expected waveform of the resulting voltage was ideally a linear function in the form of: $y = a.x + b$. The voltage theoretically comprises a current-independent part (except for the heating effect induced by the current), namely the Seebeck voltage, and a current-sensitive part, namely the resistive voltage. Therefore, the y-intercept is to be interpreted as the Seebeck voltage, being equal to $-\alpha\Delta T$, and the slope of the linear function

would represent the resistivity, R.

In brief, by sweeping a current through the device and measuring the voltage, one can retrieve both the resistance and the Seebeck voltage, by a linear fitting.

Two attempts were performed on Device 1 at -40°C, with a positive current sweep, and a negative current sweep to assess roughly the robustness of the present method.

The temperature difference across the sample during both sweeps was 0.8 K. Table 5.1 sums up the results with this technique as compared to the more traditional method (alternating current polarity) primarily used for this work.

Table 5.1: Current sweeps vs. Alternating Current Polarity method for Device 1 at -40°C

	Positive sweep	Negative sweep	Trad. method
α (μV/K)	-144	-152	-144
R (Ω)	22.1	27.8	28.3

Table 5.1 shows that the current sweep method provides results in the vicinity of these obtained by alternating current polarity. The Seebeck coefficient presents errors lower than 6% of the current sweep with respect to the alternating current polarity method. Similarly, resistance values exhibit errors below 22%. Statistically comparing the two methods, regarding the Seebeck coefficient, the current sweep method provides a standard deviation of 6.18 μV/K against 15.5 μV/K (average standard deviation) for the traditional method. Similarly, the resistance values are found to yield a standard deviation of 4.03 Ω versus 3.44 Ω (average standard deviation) for the traditional technique.

Robustness-wise, the results of the current sweeps seem to be equivalent to those obtained with the alternating current polarity method. However, it must be stressed that only two current sweeps were performed, and only a single device. Therefore the statistics presented above should be taken into account carefully. They only show the potential use of this method at a larger scale, along with a range of of standard deviations that should be obtained. Further use may

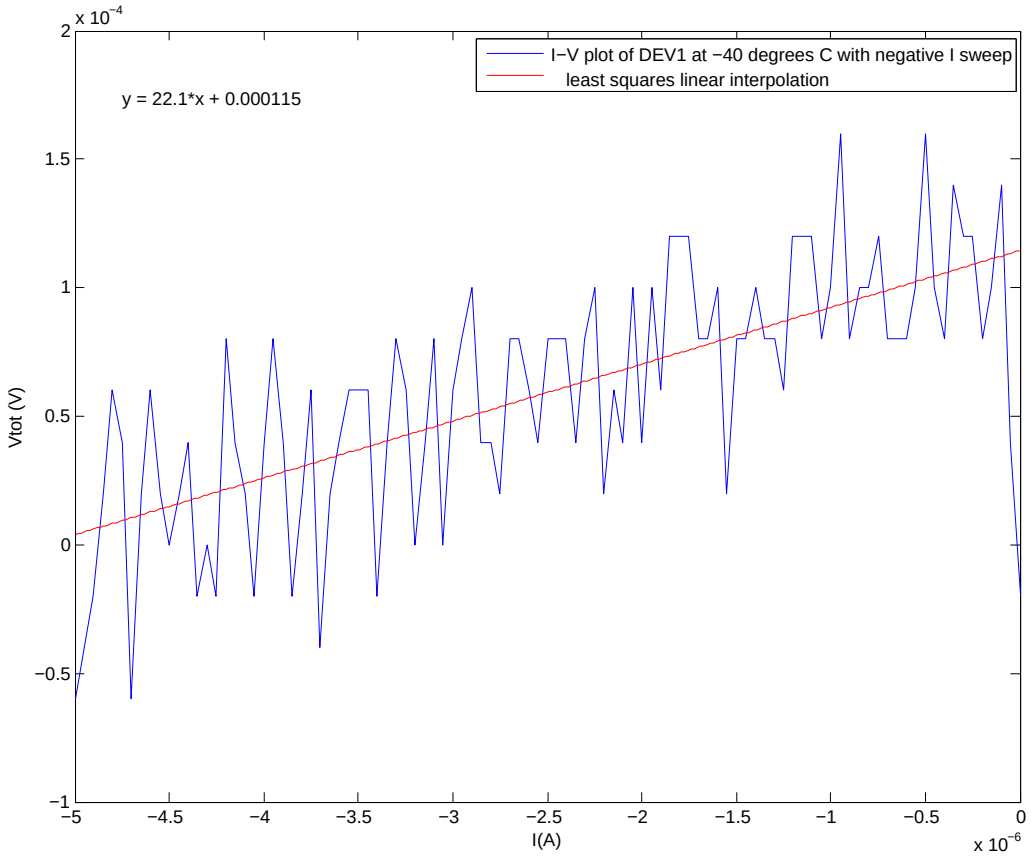

Figure 5.1: Negative current sweep – Device 1 at -40°C

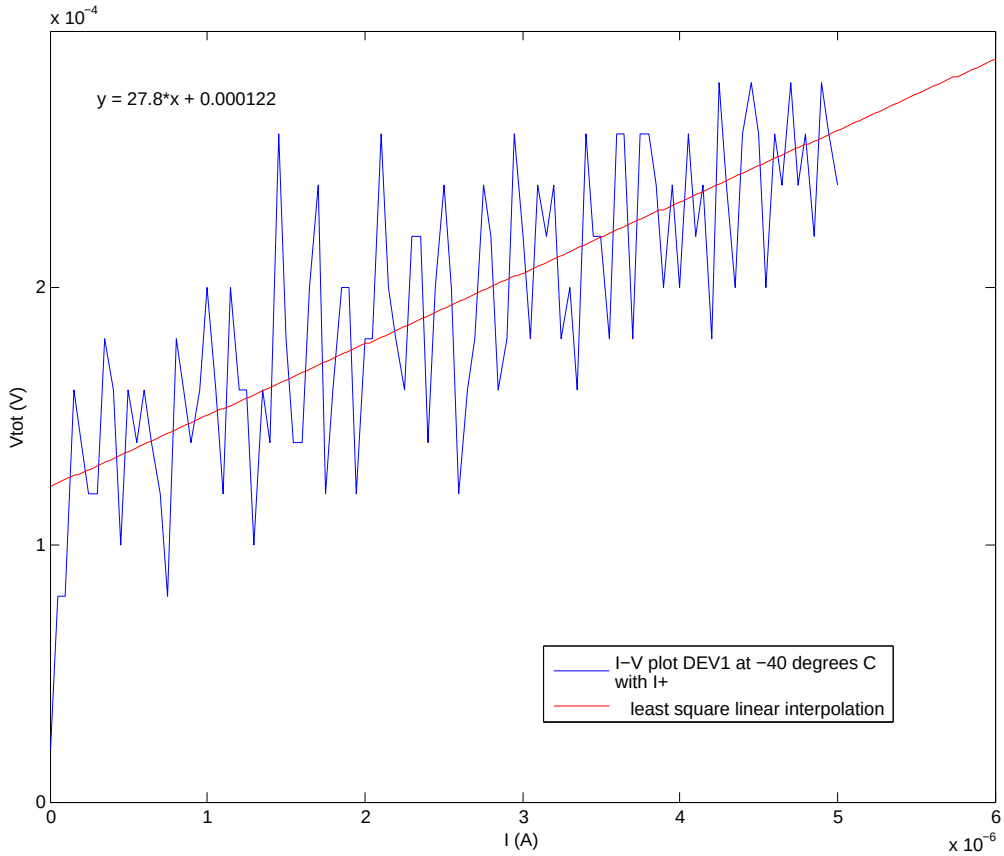

Figure 5.2: Positive current sweep – Device 1 at -40°C

confirm the validity of this method. This will be duly reminded in Section 6.2 along with other recommendations for future work.

5.2 Results and Discussion

In the measurement and calculation of the Seebeck coefficient, a critical parameter is the temperature across the device of interest (ΔT). Since this factor is generally small (about a degree or less), seemingly irrelevant variations in the display of any thermometer can in fact result in a great change of Seebeck coefficient. Following the results plotted below, a first-cut analysis is performed so as to assess the quality of this important parameter. As for the voltage signals, they appear in the equation for α in the numerator, in the form of $(V^+ + V^-)/2$ or $\Sigma V/2$ as in the tables. The voltage signals appear in the form of a subtraction in the calculation of the resistance in the form of $(V^+ - V^-)/2$, in the numerator. Adding this to the table would overload it as this is proportionally impacting the resistance value already displayed. Although the variations in the numerator are less serious than at the denominator, it remains important to analyze them. These two sources of instability (voltages and temperatures) cause the error in the values of α and R, which may also be commented. The possible reasons for such changes will be further discussed after following the analysis. Nevertheless, the most reliable sets of measurements would show a stable $(V^+ + V^-)/2$ (ensuring a stable α), a stable $(V^+ - V^-)/2$ (ensuring a stable R), and a stable ΔT, also ensuring to a large extent the correctness of α.

If the mean of the voltages, and their difference, are supposed to be stable, it is mathematically equivalent to expecting the signals themselves to be stable. In other words, provided that α and R are supposed to be stable in time (i.e. not affected by the measurement) then it should be expected that the maximum and minimum voltages of a cycle (V^+_{mean} and V^-_{mean}) are stable from a cycle to another. This consideration provides an interesting criterion (to be tested) to answer the question "How many cycles are necessary and sufficient?". Of course,

thermal stability adds to this criterion. These two criteria will be mentioned in the recommendations for future work on page 119.

Also, in the tables that will follow, the temperature stability will be summed up through the use of three indicators, namely ΔT_{min}, ΔT_{max} and ΔT_{mean}. They respectively represent the lowest, highest, and average temperature difference across the sample, over the 6 half-cycles that characterize a measurement set.

5.2.1 Analysis of the control device signals

Table 5.2: Measured and calculated data for Control device at -40°C

	I^+ (μA)	I^- (μA)	V^+_{mean} (μV)	V^-_{mean} (μV)	$\Sigma V/2$ (μV)	ΔT_{min} (K)	ΔT_{max} (K)	ΔT_{mean} (K)	α (μV/K)	R (Ω)
Cycle 1	5	-5	228	40	134	0.7	0.6	0.65	-206	18.8
Cycle 2	5	-5	251	35	143	0.7	0.7	0.7	-205	21.6
Cycle 3	5	-5	248	87	167.5	0.7	0.7	0.7	-239	16.1

Table 5.2 shows relative voltage stability in the two first cycles, while there is an increase in the third cycles, especially in its second half-cycle. Temperatures are particularly stable in the second and third cycles. Therefore, the most reliable cycles are the second for α and the first and second for R since temperature differences do not affect R.

Table 5.3: Measured and calculated data for Control device at +40°C

	I^+ (μA)	I^- (μA)	V^+_{mean} (μV)	V^-_{mean} (μV)	$\Sigma V/2$ (μV)	ΔT_{min} (K)	ΔT_{max} (K)	ΔT_{mean} (K)	α (μV/K)	R (Ω)
Cycle 1	5	-5	163	17	90	-0.5	-0.6	-0.55	163	14.6
Cycle 2	5	-5	205	17	111	-0.6	-0.6	-0.6	185	18.9
Cycle 3	5	-5	168	19	93.5	-0.4	-0.5	-0.45	212	19.1

Table 5.3 shows similar voltage signals in the first and third cycles, while there is an increase in the second cycle, especially in its first half-cycle. Temperatures are particularly stable in the second cycle, with relatively little variations for the first and third cycles. Therefore, since no cycle exhibits both stable voltages and temperature, this set of measurement does not have any cycle that is more reliable than others.

5.2.2 Analysis of DEV1 Signals

Table 5.4: Measured and calculated data for Device 1 at -40°C

	I^+ (μA)	I^- (μA)	V^+_{mean} (μV)	V^-_{mean} (μV)	$\Sigma V/2$ (μV)	ΔT_{min} (K)	ΔT_{max} (K)	ΔT_{mean} (K)	α (μV/K)	R (Ω)
Cycle 1	5	-5	247	-34	107	1	0.9	0.95	-112	28.1
Cycle 2	5	-5	278	13	146	1	0.5	0.75	-194	26.5
Cycle 3	5	-5	240	-62	89	0.8	0.6	0.7	-127	30.3

Table 5.4 shows little stability in either voltages or temperatures. Temperature instability is in fact extremely high for this set. The least impacted cycle is Cycle 1. Moreover the change in the value of R is insignificant. Therefore, Cycle 1 is by default the most reliable cycle for α and R.

Table 5.5: Measured and calculated data for Device 1 at +40°C

	I^+ (μA)	I^- (μA)	V^+_{mean} (μV)	V^-_{mean} (μV)	$\Sigma V/2$ (μV)	ΔT_{min} (K)	ΔT_{max} (K)	ΔT_{mean} (K)	α (μV/K)	R (Ω)
Cycle 1	5	-5	153	87	120	-0.9	-1	-0.95	126	6.6
Cycle 2	5	-5	185	53	119	-0.8	-0.8	-0.8	149	13.2
Cycle 3	5	-5	102	86	94	-0.6	-1.2	-0.9	104	1.6

Table 5.5 shows little stability in all cycles. Temperature-wise, extreme instability is found in Cycle 3 (variation of 0.6°C) , while Cycle 1 is relatively stable and Cycle 2 is perfectly stable. Cycle 2 will therefore by default be the most reliable cycle for α only. As for R, there is no obvious preference for any cycle considering the voltage instabilities. It is wiser to consider the average. Similar treatment will be applied to signals with no most reliable cycle.

5.2.3 Analysis of DEV2 Signals

Table 5.6: Measured and calculated data for Device 2 at -40°C

	I^+ (μA)	I^- (μA)	V^+_{mean} (μV)	V^-_{mean} (μV)	$\Sigma V/2$ (μV)	ΔT_{min} (K)	ΔT_{max} (K)	ΔT_{mean} (K)	α (μV/K)	R (Ω)
Cycle 1	5	-5	156	33	95	0.9	0.9	-0.9	-105	12.3
Cycle 2	5	-5	137	59	98	0.9	0.9	0.9	-103	7.9
Cycle 3	5	-5	148	95	121.5	0.9	0.9	0.9	-135	5.3

Table 5.6 shows good stability in the first half-cycles (V^+_{mean}) of the voltage signals, while an increase is observed with time in the second half-cycles. Tem-

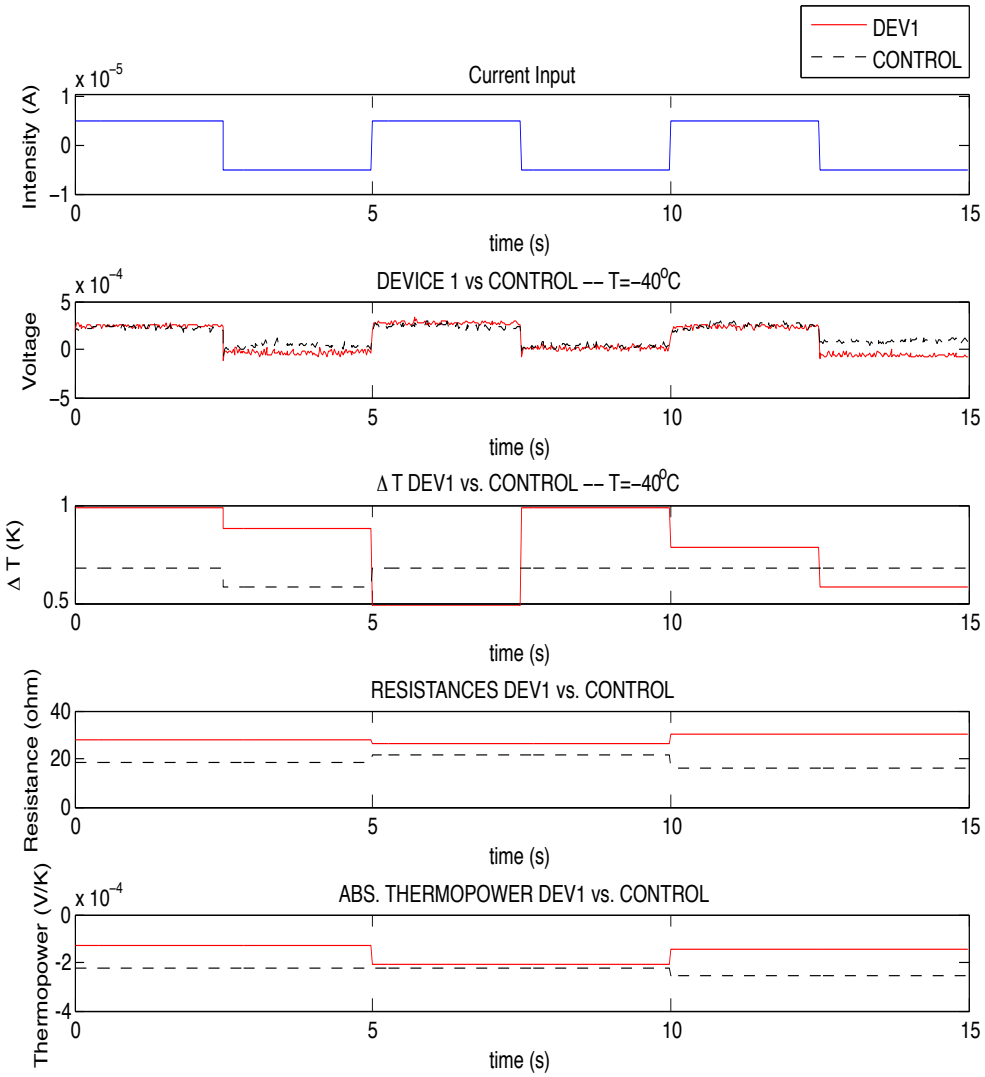

Figure 5.3: Device 1 vs. control device at -40°C

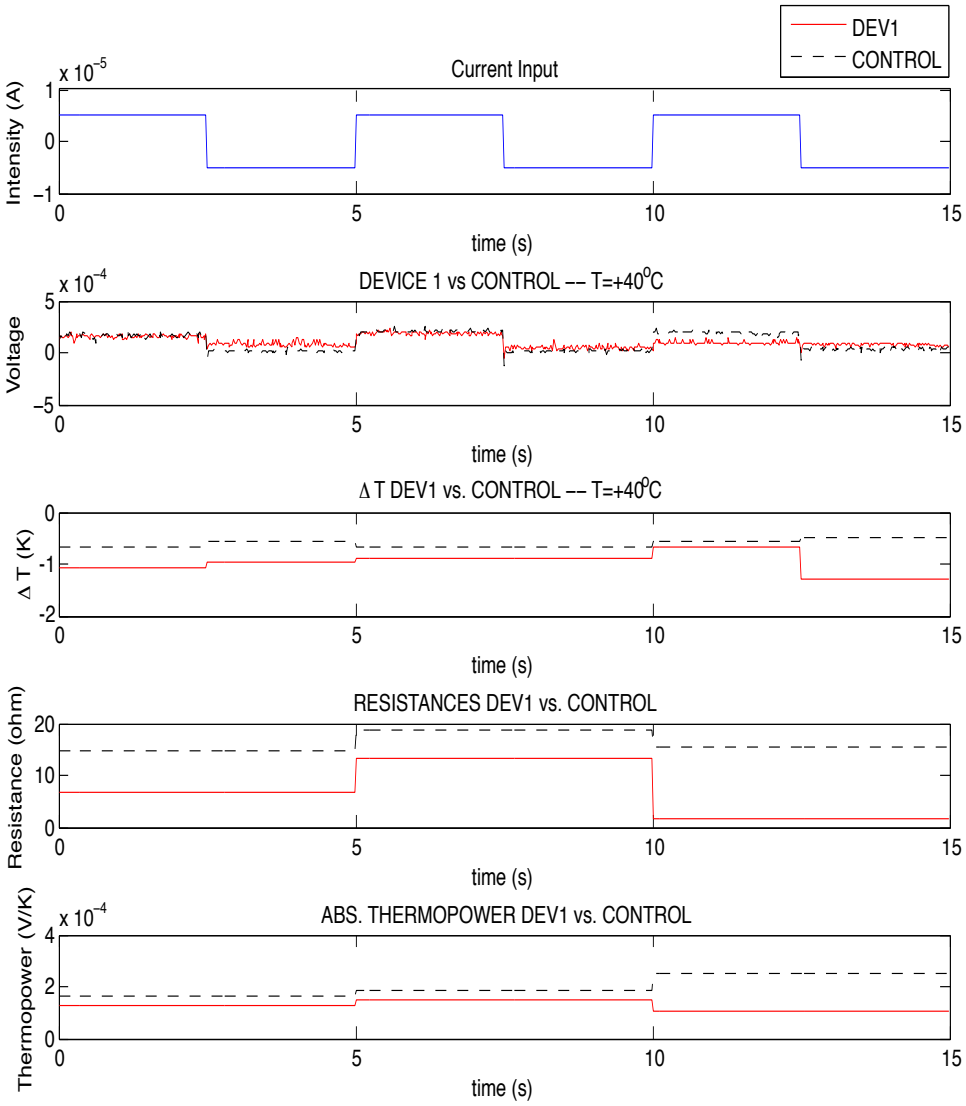

Figure 5.4: Device 1 vs. control device at +40°C

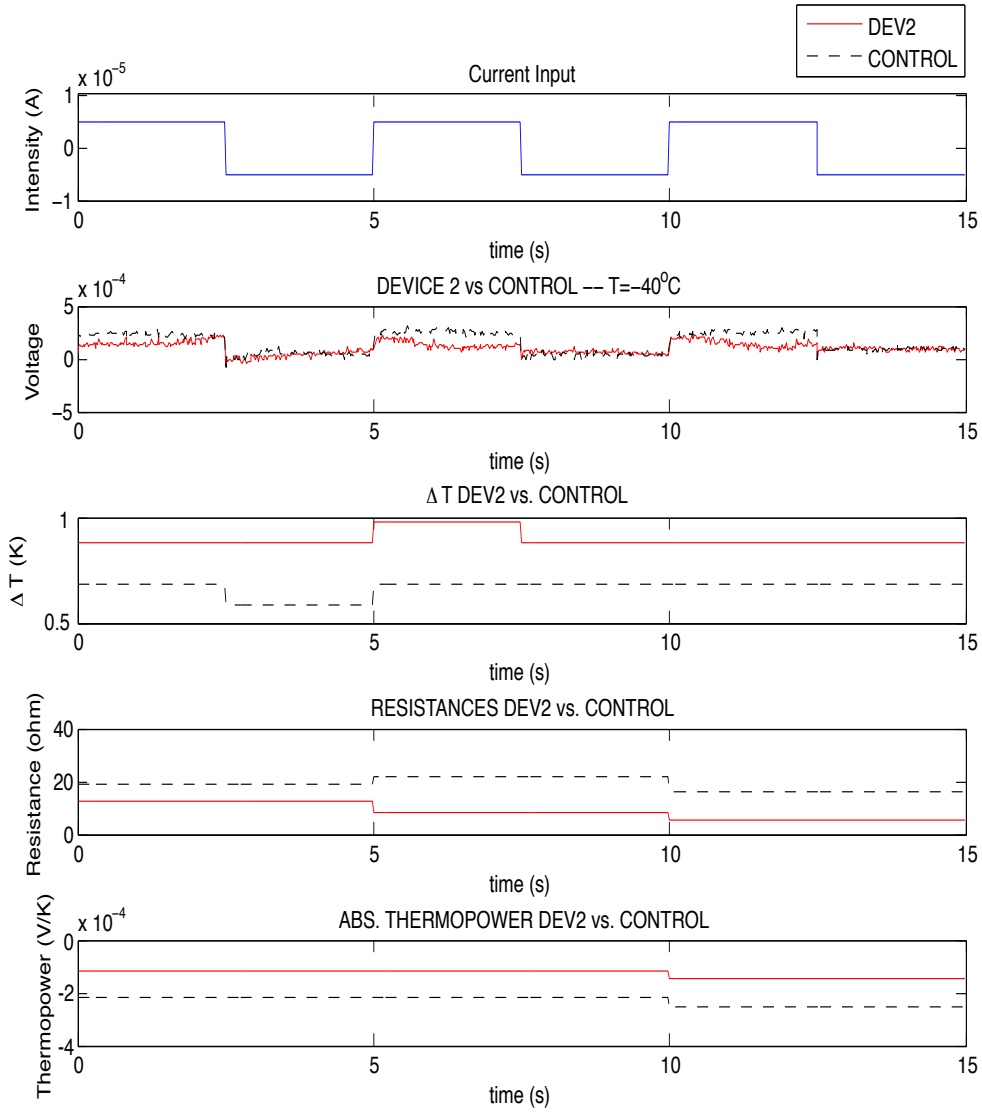

Figure 5.5: Device 2 vs. control device at -40°C

peratures are perfectly stable (as displayed with precision of 0.1 °C). Despite this fact, the voltages being unstable, there is no cycle of preference.

Table 5.7: Measured and calculated data for Device 2 at +40°C

	I^+ (μA)	I^- (μA)	V^+_{mean} (μV)	V^-_{mean} (μV)	$\Sigma V/2$ (μV)	ΔT_{min} (K)	ΔT_{max} (K)	ΔT_{mean} (K)	α (μV/K)	R (Ω)
Cycle 1	5	-5	225	18	122	-0.2	-0.2	-0.2	-608	20.8
Cycle 2	5	-5	146	24	86	-0.1	-0.1	-0.1	-852	12.2
Cycle 3	5	-5	214	66	140	0.1	0.2	0.15	-935	14.7

Table 5.7 presents very unusual temperature data. Although they are relatively stable within and across cycles, their values are extremely low compared to the usual temperature differences observed in the two other devices exposed to the same chuck temperature of +40°C. The expected temperature difference ranges around 0.55-0.85 K as found in DEV1 and the control device. Voltage signals however, although only slightly unstable in the whole, yield values that are within the usually encountered range. It is particularly unfortunate that the temperature error has occurred in this set of measurement, as previous temperature differences observed in all data showed that the temperature gradient is higher in the devices with Ge NWs as compared with the control device. A similar incident, however obvious, occurred during a measurement led prior to that presented here. The cause of temperature instability was merely the low level of battery inside the thermocouple conversion block. These were changed with high-quality brand new batteries prior to the set of measurement hereby presented, along with the batteries of the multimeters used for display.

Since DEV1 and DEV2 had comparable temperature gradients at -40°C, the temperature gradients of DEV1 will be used to estimate what the α values should have been for this set at +40°C. Had these temperatures been the same as those observed for Device 1 at +40°C, typically -0.8°C, the α values for Cycle 1, 2 and 3 would have respectively been: 153, 108 and 175 μV/K. This is in the range of usual Seebeck coefficient values.

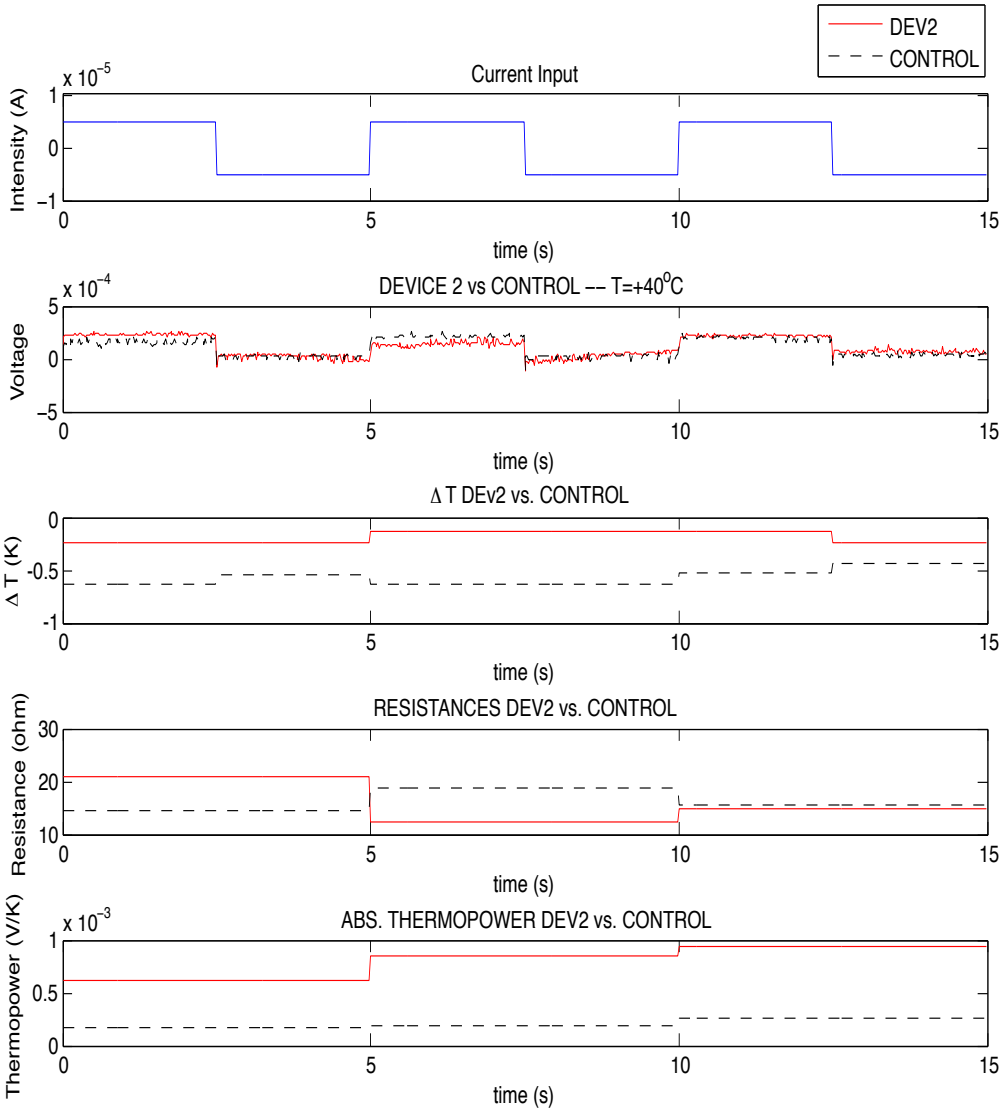

Figure 5.6: Device 2 vs. control device at +40°C

5.2.4 Summary of data

Table 5.8: Statistics on α and R on all devices, at all temperatures

	T=-40°C				T=+40°C			
	α_{mean} $(\mu V/K)$	α_{std} $(\mu V/K)$	R_{mean} (Ω)	R_{std} (Ω)	α_{mean} $(\mu V/K)$	α_{std} $(\mu V/K)$	R_{mean} (Ω)	R_{std} (Ω)
Device 1	-144	36	28.3	1.5	126	18	7.1	9.8
Device 2	-114	15	8.5	2.9	798	139	15.9	3.6
Control device	-217	16	18.9	2.2	200	3.8	16.3	1.8

Table 5.8 shows the statistical analysis of the raw measured data. It presents averages and standard deviations and does not take into account any data pre-selection. For data that was initially selected before summary, the reader is invited to refer to Table 5.9 below.

Table 5.9: Summary of α and R values **after signal selection and correction**

	T=-40°C				T=+40°C			
	α_{mean} $(\mu V/K)$	α_{std} $(\mu V/K)$	R_{mean} (Ω)	R_{std} (Ω)	α_{mean} $(\mu V/K)$	α_{std} $(\mu V/K)$	R_{mean} (Ω)	R_{std} (Ω)
Device 1	**-112**	n/a	**28.1**	n/a	**149**	n/a	7.1	9.8
Device 2	-114	15	8.5	2.9	**145**	n/a	15.9	3.6
Control device	**-205**	n/a	20.1	n/a	200	3.8	16.3	1.8

Table 5.9 shows the statistical analysis of the data after a careful selection of most reliable data sets, and estimations of the expected values for the set with unusual temperatures (DEV2 at +40°C). The values in bold font are those that underwent a correction based on the analysis presented previously.

5.2.5 Discussion on contribution of individual components within the device structure

Resistance

Copper (Cu) The resistivity of copper at room temperature is 1.7×10^{-8} Ω.cm [106]. Considering the dimensions of the copper substrate (2.5×2.5×0.2 cm), its resistance at room temperature is 5.4 $\times10^{-10}$ Ω. Although this value may differ with temperature, it remains trivial that this part of the device does not con-

tribute significantly to the resistance of the whole device. **It must be reminded that the resistance values that were measured range in the tens of ohms**.

p-doped silicon (p-Si) The resistivity of the silicon substrates used in the device is in the range of 0.85-1.15 Ω.cm. Considering the dimensions of a sample (1×1×0.0275 cm), its resistance is in the range of 23-32 mΩ. The contribution of the silicon substrate to the device's resistance is therefore insignificant.

Silicon oxide SiO_2 The SiO_2 thin film present in the device forms an MOS device as it is formed above a silicon sample and topped with a thin gold film. The SOG that we used is based on methyl siloxane. Based on methyl siloxane resistivities found in the literature [107], the oxide layer used in the experimental devices should have a resistance above 2.86×10^{10} Ω, and a resistivity above 5.71×10^{14} Ω.cm for a film with a thickness of 500 nm. The resistance of the SOG layer is highly dependent on whether defects are present.

Germanium nanowires The resistivity of Germanium NWs will be calculated by assumption that it is the same as that found in nanoporous germanium. From reference [108], the resistivity can be deduced from the power factor ($S^2\sigma$) knowing the Seebeck coefficient range. A resistivity range of $0.84\text{-}1.89\times10^{-2}$ Ω.cm was found. Using the classical bulk formula to calculate the resistance of a single nanowire would not be appropriate as it well known that this formula does not apply to the nanoscale world. Besides, the knowledge of the resistance of a single wire would not yield exploitable information as the focus is the resistance of the whole array of nanowires. As expected, the resistivity is found to be a lot smaller than that of the SOG thin film.

Conclusions on the device's resistance The vertical stacking of the layers in our devices allows us to use a series model to estimate the total resistance. A device without NWs is expected to have a resistance above 2.86×10^{10} Ω. In the case

of devices with NWs, the NWs will likely decrease the resistance of their embedding oxide film, although this is again highly dependent on whether defects will alter the expected trend.

Seebeck coefficient

Copper (Cu) The Seebeck coefficient of copper is extremely low as it is of about 1μV/K at temperatures from 10 to 300K [109]. The maximal temperature that is used in this study is +40°C, relatively close to room temperature, the Seebeck coefficient is not expected to be significantly larger for such little temperature shift. Thus, the Seebeck contribution of the copper bottom of the device is relatively little, if not insignificant. At a chuck temperature of -40°C, the top copper temperatures for all devices was about -32°C. Thus, supposing that the temperature gradient occurs entirely within the copper, this induces at worst a voltage contribution of about 8 μV. At a chuck temperature of +40°C, the gradient within the copper is only about 1K, resulting in about 1μV of voltage contribution. In brief, the contribution of the copper plate in the device structure is fairly low (from about 1 to 10%) of the total Seebeck coefficient. This, again, is provided that the whole gradient occurs within the inside of the copper plate. In practice, the copper contribution is expected to be lower since the air interface between the copper bottom and the chuck is likely to have caused a significant part of the temperature difference.

p-doped silicon (p-Si) The silicon sample is p-type, with a boron concentration of 1-2$\times 10^{16}$ cm^{-3}. The Seebeck coefficient for p-type silicon (boron-doped) was published [101] for various doping concentration. The closest doping concentration to that of our substrate is 2.6$\times 10^{16}$ cm^{-3}. For this value, the Seebeck coefficient of the silicon sample is about 700 μV/K at -40°C and about 400 μV/K at +40°C. The variation of the Seebeck coefficient with doping at these temperatures is almost nil. Further investigation on the effect of doping and temperature on the Seebeck effect in silicon can be found in reference [101]. Considering the

low temperature gradients across the silicon sample (less than 1°C), such Seebeck values may generate voltages of 400 to 700 μV. The Seebeck contribution of the silicon sample is important.

Silicon oxide SiO_2 The Seebeck coefficient of silicon oxide was not found in the literature. However, as a dielectric, it is expected to have poor thermoelectric performance like many of the classic oxides. Recent studies on a new branch of thermoelectric materials have observed that a specific engineering of oxides can lead to Seebeck coefficients higher than 100 μV/K [110]. The study mentions "*Most importantly, $NaCo_2O_4$ has relatively low mobility of 13 cm^2/V.s (at 300 K), which is strikingly against* ***the common sense that a low-mobility conductor cannot be a thermoelectric material***". It can be induced from this, at least qualitatively, that common oxides with no particularly advanced structures may have Seebeck coefficients significantly lower than 100 μV/K.

Germanium nanowires Since the Seebeck coefficient of Ge NWs has solicited interested only very recently, virtually no data is available on the subject. As a consequence, it will be assumed that Ge NWs have the same Seebeck coefficient as nanoporous germanium. It will also be assumed that the Ge NWs that are grown onto the silicon samples have the same doping as the substrate, 1-2$\times 10^{16}$ cm^{-3}. Recent theoretical models predict that the Seebeck coefficient of n-type nanoporous Ge is of -150 to -300 μV/K for a doping concentration of 5×10^{17} cm^{-3} [108]. No data is available for lower concentrations, nor for p-type nanoporous Ge. However, linear extrapolation suggests values in the range of -400 to -600 μV/K for our range of doping, yet for n-type. Assuming that the p-type equivalent device, with the same doping concentration has a Seebeck coefficient of the same magnitude and with an opposite sign, yields a Seebeck coefficient of 400 to 600 μV/K.

Conclusions on the device's Seebeck coefficient The total cross-plane Seebeck coefficient in a given device can be added provided that they all are of the same sign, otherwise they cancel each other [111]. In our case it is likely that the signs of the major contributors to the Seebeck effect (silicon sample and germanium nanowires) are identical, more specifically of positive sign, since holes are the majority charge carriers for p-type silicon. Only the sign of the oxide's Seebeck coefficient is unknown, but its value seems negligible, or at least not prominent. Qualitatively, a total Seebeck coefficient of about 400 to 700 μV/K is expected without NWs. These values may vary slightly depending on the doping and the Seebeck coefficient of the oxide. Besides, the data regarding the Seebeck effect of germanium suggests that the germanium contribution may be detectable. It also suggests that this contribution may not exceed a few hundred microvolts per kelvin. This is supported by two independent studies, in which n-type Si/Ge composites (superlattices [100] and oxide-embedded quantum dots [98]) show respectively Seebeck coefficient values of -229.6 +/- 10 μV/K and about -300 μV/K at room temperature, with similar thicknesses as in our study (about 100-1000 microns). Ref [98] also shows that the Seebeck coefficient increases more or less linearly around room temperature, with an increase of 120 μV/K from measurements performed at -40°C to +40°C (for an n-type nanostructured Ge material). It will be assumed again that the same doping concentrations with a p-type material would yield an opposite Seebeck coefficient and that the Seebeck coefficient decreases by 120 μV/K from -40°C to +40°C. Besides, in our study, the silicon substrate participates in the measurement circuit and its contribution must be taken into account. The Seebeck coefficient of silicon alone is expected to decrease from 700 to 400 μV/K at these same temperatures.

As a consequence, for devices with NWs, at -40°C, the global Seebeck coefficient is expected to be 700 + a few hundreds due to the Ge NW contribution, and it is expected to decrease by approximately 420 μV/K at +40°C due to the changes in the Ge NW and Si substrate Seebeck effect with temperature. As for

reference devices, therefore without Ge NWs, the global Seebeck coefficient is expected to be about 700 μV/K at -40°C and decrease of 300 μV/K at +40°C.

5.2.6 Discussion of results

The following discussion aims at comparing the experimental results with theoretical predictions but also with each other. These comparisons will exclusively rely on the table summurizing the α and R values after signal selection and correction (see Table 5.9 on page 100).

Experiment vs. Theory

General observations For all devices, the first comment concerns the order of magnitude of the Seebeck coefficient values. Experimental values range in the vicinity of -200 to 200 μV/K while theoretical considerations predicted values of 400-700+ μV/K, which are not within the same order of magnitude.

The Seebeck coefficient of all devices increase of about 200 to 400 μV/K with an increase in temperature, whereas they were expected to decrease of about the same values as temperature increases.

Additionally, the control device show a higher Seebeck coefficient difference with an increase in temperature, whereas it was expected to exhibit a lower Seebeck coefficient difference than DEV1 and DEV2.

The experimental mismatches with expectations may essentially be due to the lack of fine precision in the measurement of the temperature difference, and partly to the hypothesises made to define the expectations.

The nature of the behaviour mismatch suggests that not only the temperature differences were not exactly faithful to reality, but the bias between measurements and reality was not constant.

Otherwise, the values may have differed, but the behaviors (change in the Seebeck coefficient value with increasing temperature) would have matched.

This important aspect will be mentioned in a further list of possible sources

of error (page 108). As for resistance, it can be noted, despite differences, that all are found to be below 30 Ω.

DEV1 vs. theory Besides the comments made earlier, the resistance of DEV1 decreases when the temperature increases, which is the expected behavior for semiconductors and insulators near room temperature.

DEV2 vs. theory The resistance of DEV2 is found to decrease with temperature. It must be noted that the measurement of resistance is independent from the precision in the measurement of temperature gradients. This peculiar behavior of DEV2 could suggest that DEV2 contains a higher density of Ge NWs. The possible reason why the Ge NWs show metallic instead of semiconducting behaviour could be due to defects in the Ge NWs. Highly defective semiconductor nanowires can show metallic behaviour.

Control device vs. theory The control device consists of the SOG layer (an insulator) without Ge NWs. Its resistance is found to decrease when the temperature increases, as expected from semiconductors and insulators near room temperature.

With vs. Without Ge NWs

General observations At -40°C, both DEV1 and DEV2 have a higher Seebeck coefficient than the control device, which supports the expectations as the use of Ge NWs is expected to increase the overall Seebeck coefficient of the device. However, this superiority of the the Seebeck coefficients of DEV1 and DEV2 over the control device is not found at +40°C. This supports the hypothesis previously made on the lack of precision in the measurement of the temperature gradient.

Additionally, at -40°C, all Seebeck coefficients are negative, whereas a relatively high positive value was expected. There are several possible explanations.

It is possible that the high-temperature growth process may have changed the doping concentration and distribution of the silicon substrate, or its thermoelectric properties. Also, resistive effects, such as contact resistance, may have impacted on the reading of the Seebeck voltage. Taking this effect into account could allow negative voltage values instead of slightly positive ones. It was not done in this study but can be achieved with 4-probe measurements, and would yield a positive Seebeck coefficient as expected from the negative-current half cycles at -40°C. Finally, the alternating current polarity method was used on a limited number of cycles. Using a larger number of cycles may allow to enter a stable regime, where voltage readings are well repeatable. In this hypothetical regime, and during negative-curent half-cycles at -40°C, one may observe negative voltages instead of small positive voltages, which again may produce a positive Seebeck coefficient as expected.

DEV1 vs. Control device The resistance of DEV1 at -40°C is higher than that of the control device. This could suggest that DEV1 contains a very low density of Ge NWs or there could be voids or delaminations within the layer containing the SOG and Ge NWs. Voids or delaminations may manifest as an increase in resistance at low temperatures as the voiding/delamination could worsen as temperature decreases.

DEV2 vs. Control device See "general observations".

SEM verification of defects

The comparison of all devices with expectations and those of DEV1 and DEV2 with the Control Device have raised two questions concerning potential defects in the NW layer and density of the NWs. It was suggested that DEV1 either has a very low density of NWs or other structural defects, such as voids or delaminations. From an independent consideration, it was also suggested that DEV2 may have a higher NW density than DEV1, thus supporting part of the previous

hypothesis saying that that the density may differ from the two samples. Otherwise, it is likely that the oxide layer in DEV1 has defects or that DEV2's Ge NWs have structural defects.

On the one hand, Figures 5.7 and 5.9 show the main views of DEV1 and DEV2 after the growth and prior to the SOG integration. No major defects are observed but it can be seen that DEV2 has an large scratch, larger than the defects on DEV1. This observation does not however confirm that DEV1 has defects. SEM micrographs of the structure after the SOG deposition and prior to the gold sputtering were not necessary, but they could have confirmed or refuted that DEV1 has voids and delaminations. On the other hand, Figures 5.8 and 5.10 show single close-up views of the nanowires present at the center of DEV1 and DEV2, respectively. It is not obvious from the micrographs that the densities differ. Although the observation is based on two single micrographs, it can be seen that DEV2's nanowires (Figure 5.10) seem more distorted than those in DEV1 (Figure 5.8). The devices were grown with the same experimental conditions. However, inside the furnace tube, the devices are next to each other. Therefore, the devices are not exposed to the exact same temperature. The distorted nanowires are in fact obtained by design in order to create opportunities to scatter phonons. The distorted aspect of the nanowires is directly linked to the growth temperature, or substrate temperature. Given the high temperature gradients along the quartz tube, the growth temperature are not the same for several samples grown in a same batch. This supports the difference in the structure of NWs between DEV1 and DEV2, and may further justify why DEV2 exhibits a metallic behaviour because of the defective (distorted) NWs.

5.2.7 Possible sources of errors

Although the measurement protocol presented in this study did successfully measure qualitatively the Seebeck effect, their precision can widely be discussed, and does not seem to allow for an estimation of the contribution of Ge NWs.

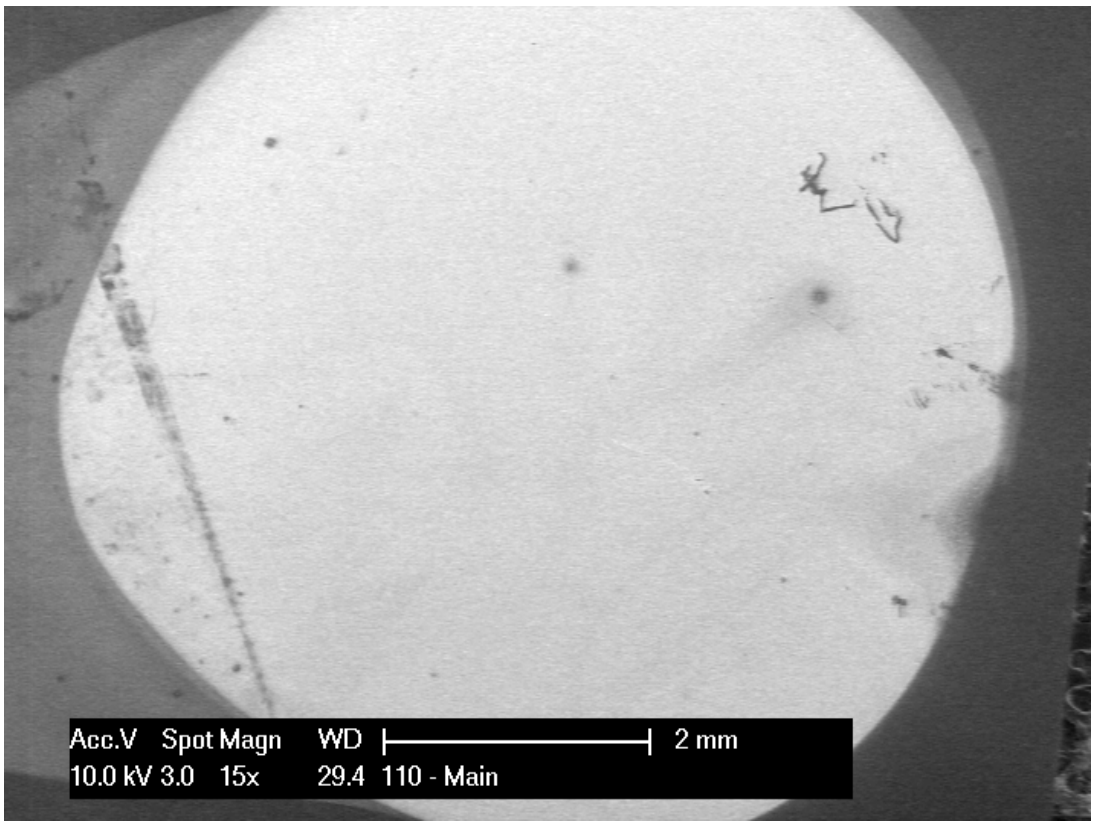

Figure 5.7: SEM view of DEV1, prior to SOG integration

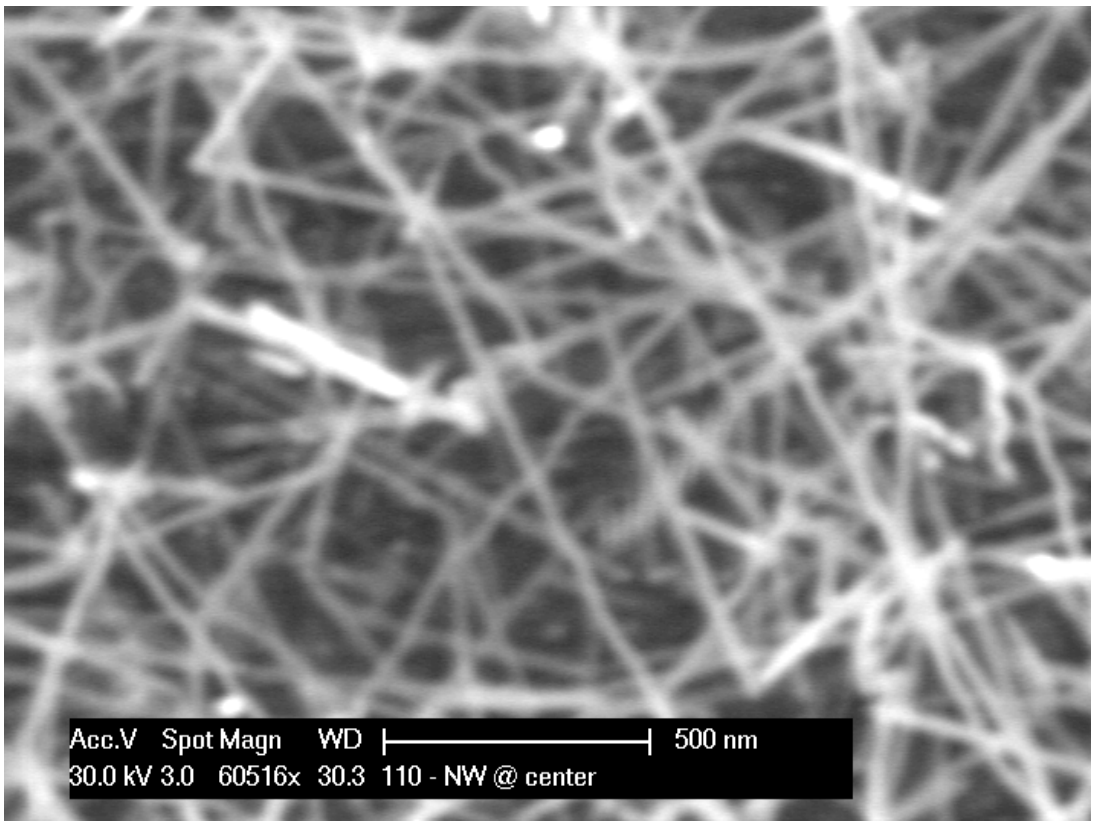

Figure 5.8: Closer SEM view of NWs in DEV1, prior to SOG integration

Figure 5.9: SEM view of DEV2, prior to SOG integration

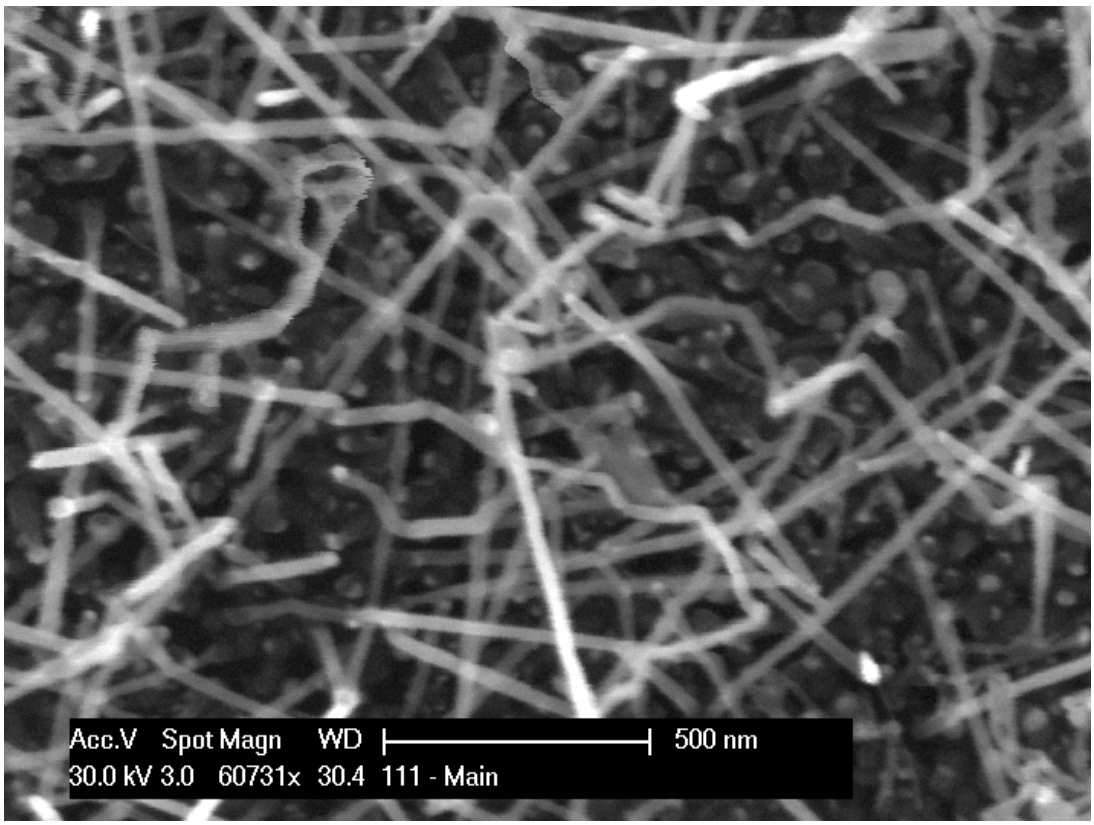

Figure 5.10: Closer SEM view of NWs in DEV2, prior to SOG integration

Indeed, at +40°C for instance, all pertinent measurements of the Seebeck coefficient seem to show values that are smaller than the Seebeck coefficient of the device that contains no NWs. The opposite effect was expected, the Seebeck coefficient values were expected to be higher. As mentioned in the earlier discussion, it is due to a large extent to the extreme difficulty in measuring a temperature difference across thin films.

Contact resistances and 4-probe measurement The measurement techniques, that were used or proposed, all require at most two probes. In such cases, resistance measurements include the contact resistances, the order of which is uncertain. To ensure that these do not affect the precision in resistance measurement, one may add a pair of probes for a passive measurement of the induced voltage. This is perfectly compatible with the above-mentioned techniques.

Precision of the current alternating polarity method First, the nature of the measurement technique is discussed. The technique hereby used is based on a differential comparison of two sets of devices, one with and the other one without NWs. Differential techniques, in general, provide clear results when the differential gains are detectable, somewhat constant, and large with respect to the base signal. Also, it was shown that the current alternating polarity method within constant experimental conditions, is rather unprecise with respect to the low order of magnitude of benefit in Seebeck coefficient that is expected from the Ge NWs, at best a few hundreds of μV/K. Since the real value, without assumptions or estimations has not been published in the literature, it could as well be very low, in which case the present current alternating polarity method would be inappropriate.

Difference in fabrication of NW device and Control Device The control device, because it contains no NW, has a flat surface and a uniform thickness, much unlike devices with NWs. The non-uniformities in the NW devices are in the

range of 100-1000 microns. No means of flattening such as CMP was available. Thus, even with ideal temperature measurement, the structures of the devices with NWs differ greatly in form with that of the reference devices.

Electrical circuitry For the sake of simplicity, the electrical circuit included the probe station's chuck (used as ground) and the copper substrate. Although it makes the measurement possible with a single probe, it was not necessary, and is in fact a source of noise, to include these in the global circuit, especially the chuck. The single probe measures the total voltage created from the parameter analyzer to the top gold layer. Therefore, this voltage corresponded to the total Seebeck effect occurring on the whole chain. This includes the chuck which is particularly subject to the Seebeck effect since it is the heating element. Additionally, the Seebeck effect also occurs at the interface between two metals, such as the interface between the chuck and the copper substrates of all devices. Ideal measurement conditions would have established the ground on device (i.e. onto the copper substrate), in order to measure exclusively the Seebeck voltage that occurs inside the device.

Parameter Analyzer's precision When used as a current source, the voltage precision of the parameter analyzer is 20μV. This means that for a temperature gradient of 1K (which is common) the precision in terms of Seebeck coefficient is 20μV/K. Unless one has precise previous knowledge of the expected value, a precision of 20μV/K is not sufficient to measure the Seebeck coefficients which could be low.

Non-simultaneousness of voltage and Temperature measurements Although the temperature were in general stable when displayed on the multimeter, these were collected "by hand", as closely in time as possible to the ongoing current sweep. During this time, the temperatures may vary. Since the Seebeck measurement was done using a sweep, it would have been preferable to collect the

temperature in the same fashion, meaning by collecting frequent data points. A way to do this would be to connect the thermocouple units directly to the parameter analyzer.

Temperature Precision: Equipment The devices that were used to measure the temperature were not specialized equipment. Although the manufacturer stated an output voltage of 1mV/K, a simple calibration test revealed that two identical units display different temperatures when placed very closely in space on a heating stage. Additionally, the correction factors that were calculated depend on temperature. No test was performed to ensure that the temperatures are stable with time. In brief, besides fabrication challenges, temperature measurement is the most critical aspect of this project. Immense care should be used in making sure that the temperature measurement devices are well calibrated and that they will yield precise results that are faithful to reality, if not in terms of absolute temperature at least in terms of relative temperatures.

Temperature Precision: Display Given that precision in the temperature measurement is absolutely crucial, it is important to ensure that these are precisely displayed. Unfortunately, the precision of the display was 0.1K, which represents for instance a 20% imprecision for a gradient of 0.5K, as it was the case in a measurement. Another benefit of connecting the thermocouple unit to the parameter analyzer would have been to utilize the analyzer's voltage precision. In this particular case, the voltage precision of the parameter analyzer would yield temperatures with a precision of $0.02^{\circ}\mathrm{C}$.

Thermal anchoring Thermal anchoring refers to the quality of the thermal link between two objects, and more precisely in our study, to the thermal link between the sample and the thermocouples. A thin layer of varnish, of uncontrolled thickness was applied to the top of the top gold thin film to ensure electrical insulation. Besides, to anchor the spherical thermocouple tips onto the flat

varnished area, thermic paste was used. The uncontrolled thickness of the varnish may be partly responsible for differences in the temperature gradient. It remains also uncertain how much paste should have been used, and surely the quantity varied from a set of measurements to another. On the one hand, very large amounts may insulate the thermocouple tip from ambient air and provide a temperature closer to that measured. On the other hand, large amounts may interfere with the thermal behavior of the device since it may change the thermal distribution in it. The ideal measurement would measure the temperature without establishing a contact with the top part of the device, where the thin film of interest is located. Unfortunately, such measurement devices were not available.

5.3 Summary

In this study, a set of measurements aiming at obtaining the Seebeck coefficient of Ge NWs embedded in an oxide matrix was performed. Amongst several possible methods, the alternating current polarity method was used, in which a symmetric current was applied to a TE circuit to generate a non-symmetric alternative voltage, from which both the resistance and the Seebeck coefficient can be extracted. Investigation on the effect of Ge NWs was based on a comparison with a reference sample, meaning that the contribution of Ge NWs was to be measured from the difference in Seebeck coefficients found in devices with and without Ge NWs, those without being called the reference or control devices.

Although this study was not able to confirm the Ge NW effect, it was able to qualitatively measure the Seebeck coefficient of a TE device. Many issues were encountered, concerning in particular the precise measurement of a small temperature gradient within a thin film structure.

6. Conclusion

6.1 Conclusion

In this study, two major aspects have been investigated, the growth and fabrication of TE-relevant Ge NWs, and a technique for measuring Seebeck coefficient. This investigation follows breakthrough findings reported in the recent literature on the increase of TE performance of Si due to nanostructuring. All growth was performed using a conventional furnace with vapour transport. Following initial growth on SS substrates, which may be ZT-relevant but yielded little NW growth, most of the growth effort was dedicated to <111> p-doped silicon substrates. It was observed that although it is possible to grow nanowires, obtaining TE-relevant integrable wires required the use of state-of-the-art knowledge in terms of growth and integration. It was found that long nanowires (few tens of microns) do not integrate well into with spun-on oxides like SOG. It was found that Ge evaporation occurs in sufficient amounts even at temperatures 100°C below the melting point. Reducing the source temperature from 920°C to 810°C reduced the growth rate, likely due to a reduction in vapour generation. This also reduced the growth duration by itself, although further experiments show that reducing the growth time directly impacts, as expected, the growth rate

by reducing it. Additionally, reducing the growth temperature (sample temperature) from 530°C to 450 °C proved to lower the growth rate, to ensure more homogenous NW length, while creating "zig-zag" shaped wires, which are expected to contribute to the wires' TE performance by scattering phonons. The diameter of the wires was also reduced from about 100 nm to 28 nm with the same 20 nm diameter gold colloid, likely by reduction of radial growth induced by the reduction of vapour flux. The decrease in NW diameter (or more generally the smallest dimension) is a critical factor in the improvement of the TE performance of virtually any nanoengineered object. Following these multiple NW adaptations, the NWs were successfully integrated into an SOG matrix, although chemical and mechanical polishing was not available in the laboratory to ensure uniform surfaces. A layer of gold made top electrical contact possible, on top of which electrical insulation was prepared to attach a thermocouple. Two devices with embedded NWs and a control device without NWs (the control device) underwent an attempt of Seebeck coefficient measurement. The measurement technique applied a symmetric alternative current through the devices at two different temperatures, -40°C and 40°C. This technique allows one to extract both the resistance and the Seebeck coefficient from the measured voltages. However, several inconsistencies were observed both by comparison to expected values and by comparison of the devices with each other. Most of these are believed to originate from difficulties encountered with the precise measurement of temperatures, and more specifically of the temperature gradient. The mismatch in the resistance values was explained by differences in the structure of the nanowires. Although seemingly simple, the alternating current polarity method used in this study, like other methods requires excellent control of the temperatures, but presents majors flaws, such as voltage instability. The comparison of the measurement results with a reference device was also problematic due to the lack of previous knowledge of the Ge NW Seebeck coefficient; in particular in our case where the reference device was different in

structure to devices with NWs. A simpler alternative to the alternating current polarity method was proposed, and was designed with the intention of yielding quicker and more reliable results since it shortcuts the issue of time-instability of the Seebeck voltage.

6.2 Recommendations for Future Work

The reader is primarily invited to consult the list of potential sources of errors that were discussed on page 108. Besides these recommendations, the following may bring insight on important points that should be considered in future work.

Number of cycles The voltage data collected in this study was often from slightly to very unstable with time. It was suggested that more steps be carried out, to verify whether the signal becomes more stable after a certain number of cycles.

Using the current-sweep method If the above does not make the signal stable with time, it is recommended in future work to use a method that does not rely on the average voltage over a half-period. For instance, the simple method introduced in this study can be further carried out in order to be tested to a larger scale and validated, refuted or improved.

Wire density It is possible that in this study, the NW length was overly reduced, to an extent that may not have been necessary to ensure SOG integration. Further work may explore longer NW lengths and density of nanowires. Since my focus was reducing the length of the NWs, I did not hesitate to lower the density to the advantage of shorter NWs.

CMP, SOG, and spin settings If possible, I highly recommend to use CMP in order to eliminate potential irregularities in the SOG thickness. Recent SOG with

high filling ability may also be explored. Another suggestion is to vary the spin settings, in case it can help obtaining a more uniform surface after integration.

Using other filling techniques In the paper on the integration of NWs (Ref [94], PECVD of SiO_2 is used and gives successful integration. It may be tested either on very short wires of a few microns first, to avoid accumulation problems, then on long and horizontal wires. The latter may not be successful but is mentioned for exploratory purpose because conclusive results would allow a high density of NWs in the oxide. Finally, note that CMP is required after deposition.

Superlattices The melting points of the Ge nanowires were found to be higher than the melting point of bulk germanium (937°C), typically by 6°C, and with a broad melting range (about 80°C) [112]. Provided that SOG is robust to high-temperature, the fabrication of supperlatices can be considered.

Measuring thermoconductivity Further research may find interest in completing the present study with thermoconductivity measurements. Several methods such as the 3ω method [113] can be used to achieve this purpose. Combining the knowledge of the Seebeck coefficient and that of the thermal conductivity, the ZT factor can be calculated, thus allowing comparison with existing devices.

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